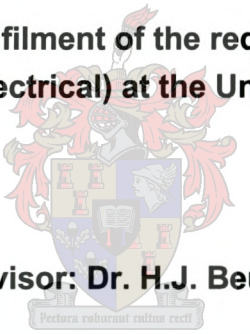
A Practical Comparison between the Three-Phase Series-Stacked and Neutral Point Clamped Multilevel Converter Topologies

G.B. Lee

Thesis presented in partial fulfilment of the requirements for the degree of Master of Engineering (Electrical) at the University of Stellenbosch



Supervisor: Dr. H.J. Beukes

October 2003

Declaration

I, the undersigned, hereby declare that the work contained in the thesis is my own work, unless otherwise stated, and has not previously, in its entirety or in part, been submitted at any university for a degree.

G.B. Lee

October 2003

Summary

The versatility of power electronic converters has made them a dominant force in the current electrical and electronic engineering industry. So too industry presents a wider range of applications, forever demanding operation at higher power levels. To meet this need a variety of multilevel converters have evolved. The challenge often lies in the selection of the appropriate topology for a specific application. This thesis presents a practical comparison between the Series-Stacked and Neutral Point Clamped multilevel converter topologies as candidates for Medium Voltage Direct Current and Traction applications. Their configurations, characteristics, switching techniques and practical performances are compared, in order to aid the topology selection process.

Opsomming

As gevolg van die veelsydigheid van drywings elektroniese omsetters word dit geimplementeer in n toenemende hoeveelheid toepassings met toenemende drywings vlakke in die elektriese en elektroniese industrie. Om aan hierdie behoefte te voorsien het n reeks veelvlak omsetters ontstaan. Die uitdaging hiermee is die keuse van die toepaslike topologie vir n spesifieke doelwit. Hierdie proefskrif vergelyk die Serie Gekoppelde en die Geklemde Neutrale Punt omsetters ten opsigte van konfigirasie, karakteristieke, skakel tegnieke en praktiese werksverrigting om die toepaslikheid te bepaal vir Medium Spanning Gelykstroom en Traksie toepassings.

Acknowledgements

In the memory of my father whose presence and advice is still sorely missed.

I would like to thank the following people and institutions:
Dr Johan Beukes for the direct guidance, encouragement and patience.
My Family members, especially my Mother, for their support and understanding.
Chantal for the many hours of personal sacrifice, her understanding and support.
Aniel le Roux, Stephan Thiel, Jacques du Toit, Niel Bester, and a host of good friends, for their guidance, patience and advice.
All my colleagues in the Power Electronics Research Group for their support and friendship.
Mr Richard Edson for backing me till the end.

ESKOM Transmission for this wonderful opportunity.

To God be the Glory

Table of Contents

List of Figures

List of Tables

List of Symbols

C_F	Filter capacitor
C_{shunt}	Shunt capacitance
δ	Load angle "delta"
d_i	Rate of change in current
d_t	Rate of change in time
d_v	Rate of change in voltage
D	Duty ratio
D_N	Diode, anode connected to negative DC rail
i	Instantaneous current
i_a	Active instantaneous current
i_n	Non-active instantaneous current
I_A	A ϕ current
I_B	B ϕ current
I_C	C ϕ current
I_{AC}	AC side current
I_{DC}	DC side current
I_{Load}	Measured load current
I_{shunt}	Measured shunt current
I_{peak}	Measured peak current
$I_{peak\text{-}peak}$	Measured peak-to-peak current
$I_{A\,P}$	Top converter's A ϕ current
$I_{B\,P}$	Top converter's B ϕ current
$I_{C\,P}$	Top converter's C ϕ current
$I_{A\,N}$	Bottom converter's A ϕ current
$I_{B\,N}$	Bottom converter's B ϕ current
$I_{C\,N}$	Bottom converter's C ϕ current
I_{NP}	Neutral point current
I_{CP}	Capacitor C_P's current
I_{CN}	Capacitor C_N's current
L_F	Filter inductor
R_L	Resistive load
S_P	Switch connected to positive rail
S_n	Switch connected to negative rail
T_{on}	Time duration with switch ON
T_{off}	Time duration with switch OFF
Ts	Switching period

u	Instantaneous voltage
V_{ac}	AC side voltage
V_{comp}	Compensation voltage
V_d	Input DC voltage
V_{dc}	DC side voltage
V_{Line}	Voltage drop over the line
V_o	Output DC voltage
V_{PCC}	Voltage at Point of Common Coupling
V_{peak}	Measured peak voltage
$V_{peak\text{-}peak}$	Measured peak-to-peak voltage
V_R	Received voltage
V_{ref}	Reference vector
V_{res}	Resultant voltage vector
V_{RMS}	Measured RMS voltage
V_S	Supply voltage
$V_{A\ P\ Conv.}$	Top converter's A ϕ output voltage
$V_{B\ P\ Conv.}$	Top converter's B ϕ output voltage
$V_{C\ P\ Conv.}$	Top converter's C ϕ output voltage
$V_{A\ Conv.}$	Converter's A ϕ output voltage
$V_{B\ Conv.}$	Converter's B ϕ output voltage
$V_{C\ Conv.}$	Converter's C ϕ output voltage
Z_{Line}	Line impedance

List of Units (SI)

A	Ampere
F	Farad, unit of measure for capacitance
G	Conductance, unit of measure for the inverse of resistance
H	Henry, unit of measure for inductance
k	kilo, demoting 10^3
M	mega, denoting 10^6
m	milli, denoting 10^{-3}
μ	micro, denoting 10^{-6}
Ω	ohm, unit of measurement for resistance
W	watt, unit of measurement of power
VA	Volt Amperes, unit of measurement of apparent power
VAr	Volt Amperes reactive, unit of measurement of reactive power
V	Volt
Z	Impedance

Glossary

APF	Active Power Filtering
DSP	Digital Signal Processor
EMI	Electro Magnetic Interference
FETs	Field Effect Transistors
FPGA	Field Programmable Gate Array
GTOs	Gate Turn-off Thyristors
HVDC	High Voltage DC
IGBTs	Insulated gate Bipolar Transistors
LVV	Large Voltage Vectors
LCD	Liquid Crystal Display
MVDC	Medium Voltage DC
MOSFETs	Metal Oxide controlled Field Effect Transistors
MVV	Medium Voltage Vectors
NPCC	Neutral Point Clamped Converter
PCC	Point of Common Coupling
p.u.	per unit
SCRs	Silicon Controlled Rectifiers
SPWM	Sinusoidal Pulse Width Modulation
SSC	Series Stacked Converter
SVM	Space Vector Modulation
SVV	Small Voltage Vectors
THD	Total Harmonic Distortion

Chapter 1 Introduction

This thesis investigates two multilevel converter topology candidates, namely the three-phase three-level Neutral Point Clamped and the three-phase two-level Series-Stacked converter topologies, as high power converter solutions for typical industry applications. Configurations, characteristics, switching techniques and performances are compared, in order to aid the topology selection process in an application, i.e. in an MVDC application or a Traction application with active power filtering and regeneration.

1.1 The Evolution of Power Electronic Converters

By definition, power electronics can be defined as the technology associated with the efficient energy conversion, control and conditioning of electric power by static means from its available input form into the desired electrical output form. Furthermore, the goal of power electronics is to control the flow of energy from an electrical source to an electrical load with high efficiency, high availability, high reliability, small size, light weight and low cost. With this in mind, power electronics can be traced back to the early 1900s [1][2], when the first mercury arc rectifier was used. Since then power electronics' development has occurred in bursts, with some devices developed, providing unexpected solutions. The biggest advancement was the junction transistor, developed in 1951 [2], which led to the development of modern power silicon switches currently being used in a vast range of industrial applications. At present four types of silicon switches are extensively used to perform the majority of power electronic conversion processes. Thyristors (SCRs), Gate Turn Off Thyristors (GTOs), MosFets (FETs) and Insulated Gate Bipolar Transistors (IGBTs), developed in the 1980s, are the workhorses in power electronics [6]. Furthermore the drive by industry to reduce emission levels, increase efficiency and conserve energy has led to extensive research on more efficient materials that have better power efficiency. Currently only about 15% of the electric power produced undergoes some form of power electronic conversion [5], while the worldwide estimated energy saving of between 15% and 20% is projected by the extensive application of power electronics [1]. One such material identified for the next generation of switches is silicon carbide (*SiC*) [1][3][4].

1.2 Power Electronic Contribution

In order to achieve insight into the two suggested power electronic solutions for two proposed high power applications, namely Medium Voltage Direct Current (MVDC) and traction applications discussed later in this section, it is necessary to review the requirements of the proposed solutions. The solutions researched in this thesis need to conform to three general requirements. They are as follows:

- High Power Ratings

- High Voltage Ratings
- High Switching Frequency

High power ratings are an area of concern since currently most power electronic solutions target the medium to low power ranges, denying high power applications the benefit of efficient operation. With regard to the high voltage requirements, high power machinery uses high voltages to reduce its losses. Power electronic solutions operating at the same voltage levels do not require extra components, potentially limiting their performance, to slot in with the required equipment. Lastly, high switching frequencies are desired since they ensure good quality waveforms and fewer harmonics, generated during switching, to occur at multiples of the switching frequency. Of the four silicon devices mentioned in the previous section, namely SCRs, GTOs, FETs and IGBTs, it can be deduced from Figure 1-1 that IGBTs are the devices that conform most to the abovementioned requirements.

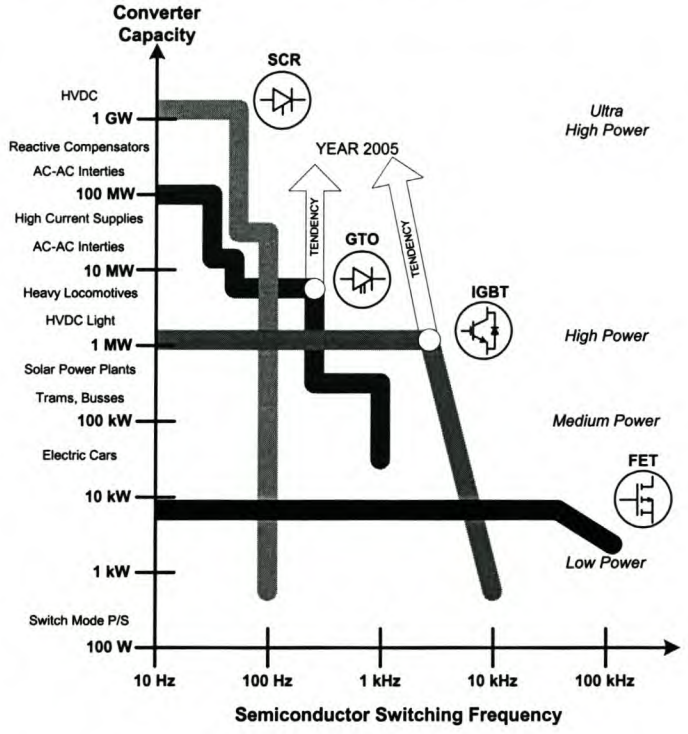


Figure 1-1: Switch Applications and Capability, Rating vs. Switching Frequency

IGBTs bridge the gap between high power ratings and high switching frequencies. They have relatively low on-state voltages, minimising losses, and in the best cases they require no snubber circuits. However, IGBTs have their power limitations, as seen in Figure 1-1. To extend their power range, a range of multi device and high voltage topologies have been developed. These range from the straightforward series connection of switches [11] to different connection configurations [7][8][9][10], all of which are discussed later in this thesis.

The two multilevel topologies investigated in this thesis are considered as candidates for the following applications, namely traction applications and MVDC power distribution. Although the converters are not applied in these applications, their performance for the required

functions in each of the applications is investigated. The enhancement and benefits of power electronic converters in the traction and MVDC applications is discussed in the following section.

1.2.1 Traction Applications

In South Africa the railway/traction system consumes a large amount of electrical energy. It is subsequently to their benefit to ensure energy efficient consumption, and then pollution of the power network is kept to a minimum. Currently a large portion of their rail network is configured to operate at 3 kV DC, typically obtained using three-phase to six-phase transformers and then rectifying the outputs using six or twelve pulse passive diode rectifiers. The ripple of the rectified DC is further smoothed by the use of a large smoothing inductor. Passive rectification, however, does not allow for bi-directional power flow.

Regeneration into the power grid, by generating electrical energy during train braking periods, is becoming a focal point in the increasing challenge of reducing operational cost. The ideal solution is shown in Figure 1-2, where the AC source voltage is transformed to DC and vice versa, allowing for bi-directional power flow. Furthermore AC line-side shunt compensation, performed by this in-line device, would be an added benefit.

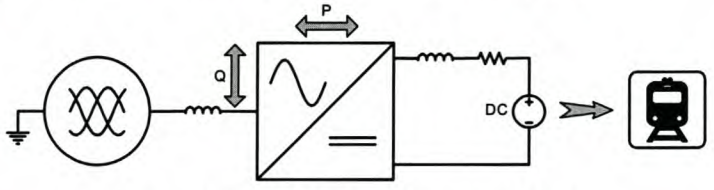


Figure 1-2: Ideal In-Line Traction Solution

A drawback to this solution is that it would require the replacement of all existing rectifiers and transformers. Passive diode rectifiers are line commutated and thus do not require any switching commands, and are regarded as a very reliable option. However, they do not permit bi-directional power flow or AC side shunt compensation. These reasons require alternative cost effective solutions to be sought, an example of which is seen in Figure 1-3.

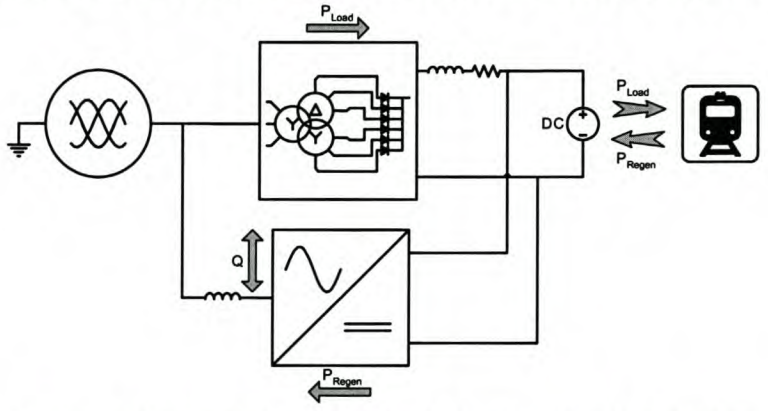


Figure 1-3: Suggested Parallel Solution for Traction Applications

The parallel connection of the DC to AC converter enables the braking energy to be regenerated into the power grid. This provides a non-intrusive solution for the diode bridge con-

figuration. It is possible to operate at reduced power ratings to that of the rectifier bridge, providing a cheaper solution than that suggested in Figure 1-2. AC line-side shunt compensation can be performed during non-regeneration periods, further reducing the rating requirements of the parallel topology. Shunt Active Power Filtering (APF) can also be employed to filter out current harmonics generated by the rectifiers. By making use of IGBT based converters and using one of the numerous multilevel topologies available, switching at these high voltage levels and the numerous functional capabilities can be realised. In conclusion, paralleling the converter to the existing topology thus permits the following capabilities:

- Power Regeneration
- Reactive Power Compensation
- Active Power Filtering

1.2.2 MVDC Applications

MVDC transmission, essentially a lower power version of High Voltage Direct Current (HVDC) transmission, has recently been receiving much attention [13][14]. MVDC has become more attractive due to recent advances in semiconductor technology. MVDC offers network planners the opportunity to bridge greater distances, using lower voltages than traditionally used in HVDC and as an alternative to medium and lower voltage AC transmission [12].

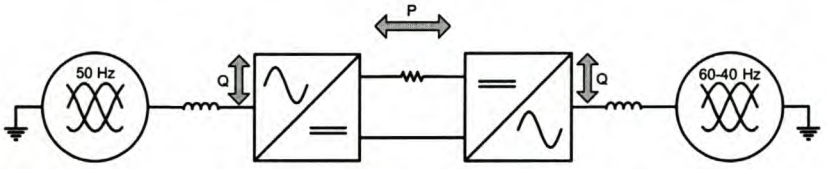


Figure 1-4: Typical MVDC Transmission Configuration

The MVDC solution, seen in Figure 1-4, provides a low loss interconnection between two AC power networks. The DC link isolates reactive power flow between the two networks, allowing only real power to be exchanged, resulting in only real power losses and no apparent power losses. The benefit of this is clear when connection is required between two power networks operating at different frequencies, say 50 Hz to a 60 Hz network. Wind farms, with varying system frequency, can also easily be connected to a fixed frequency power network via an MVDC link. The gains in using IGBT medium voltage converters as opposed to high voltage thyristor converters typically used in HVDC transmission are obvious when considering their capabilities. By actively rectifying the AC voltage, using IGBT technology, the system voltage is not polluted, as is the case for the line commutated thyristor technology. The IGBT converters are also capable of performing reactive power compensation with their excess capacity, whereas the traditional thyristor based technology isn't. Active power filtering on the network can also be realised, while still converting AC power to DC power. By connecting the MVDC feeder in parallel to other AC power lines, like that seen in Figure 1-5, a whole range of power flow capabilities becomes available.

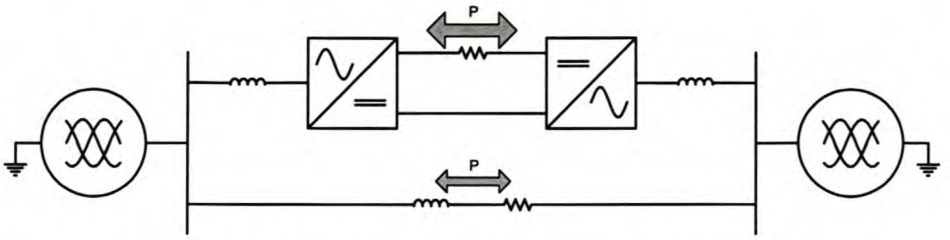


Figure 1-5: Parallel MVDC and AC Feeder Combination

Power system support, fault suppression, power flow control between utilities and the power contribution of the different lines for operation at different loading conditions are but a few examples. In conclusion, an MVDC application offers the following system capabilities:

- Low Loss DC Power Transmission
- Reactive Power Compensation
- Active Power Filtering
- Extensive Power Flow Control in Parallel Configurations

1.3 Thesis contributions

In summary this thesis investigates two specific topologies. They are the three-phase three-level Neutral Point Clamped (NPCC) and the three-phase two-level Series-Stacked Converter (SSC), chosen because of:

- The two topologies' are the best choices for this application.
- The topologies' structural simplicity.
- The need to investigate switching techniques.
- The need to obtain further knowledge on each topology's performance.

Both converters employ the same number of switching devices and have structures that facilitate the reconfiguration between both topologies, using the same components, thus enabling comparative studies to be performed. The performance of the converters is evaluated as possible candidates for two possible industrial/utility applications. The emphasis lies not in the applications but rather in their ability to perform the required functions that enhance the applications.

These applications are:

- MVDC applications primarily used to stretch a utilities power network.
- Traction applications, where the converter provides active power filtering, as well as regeneration into the grid, an attractive alternative to the current railway network operation in South Africa.

Both topologies are analysed, the design parameters considered and their control techniques compared and evaluated. The impact on specific components within the converter structures is also investigated, efficiencies determined and suitability to the various applications determined.

Chapter 2 Analysis of IGBT Converter Operation

In Chapter 1 the thesis objectives indicated that two specific multilevel topologies are to be investigated, with regard to their practical performance, as potential candidates for traction and MVDC applications. To realise this, a thorough understanding of IGBT based converters is required. This chapter investigates the basic converter operational capabilities, specifically inverting and rectifying operation. These functions equip the converter with the tools to perform a various energy compensation and conversion within a power network. Specific network phenomena and the mitigation thereof, as well as high power, multilevel applications are dealt with in later chapters. The ultimate aim in this chapter is to form a picture of the basic operation and switching techniques. The operational analysis is performed iteratively, from single-phase operation to three-phase operation.

2.1 Basic Converter Components

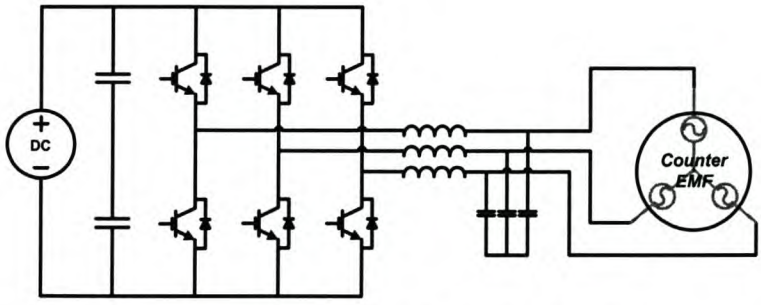


Figure 2-1: A Three-Phase Converter Structure

The standard three-phase converter, seen in Figure 2-1, consists of three separate phase-arms, connected in parallel. Each phase-arm is capable of single-phase converter operation and requires a certain number of fundamental components to operate. The components, illustrated in Figure 2-2, can be categorised in three groups, namely the energy storage devices, switching devices and the filter components. The combination of these components is used to convert DC power into usable AC power and vice versa.

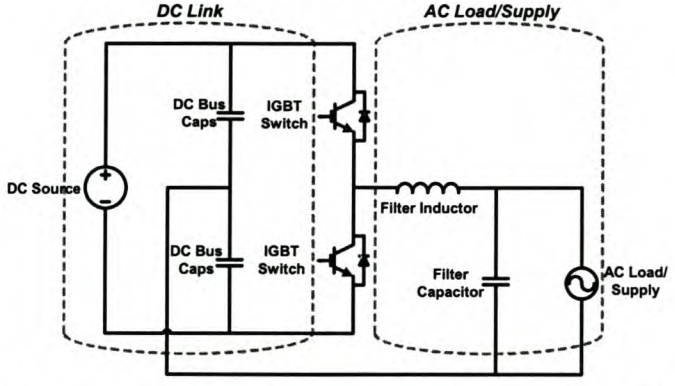


Figure 2-2: Fundamental Components of a Single-Phase Arm in a Converter

The DC bus capacitors form the energy storage component of the DC-link. Their function

is to supply or absorb ripple current flowing to and from the AC side. Switching within the converter is performed by the IGBTs, forming the interface devices between the DC and AC power. The filter inductor performs two tasks: one as a current storage device and the other as low pass filter, formed in conjunction with the filter capacitors. They provide a low impedance path for the high-frequency currents to be reflected back to the converter. Controlling these fundamental components, in the appropriate manner, allows for the modulation of nearly any kind of waveform from the DC bus. An extra phase-arm enables full-bridge switching operation, a configuration being dealt with later in this chapter, while the addition of two phase-arms enable three-phase operation. The next section describes the converter operational modes, starting at the single-phase half-bridge operation, thereafter the full-bridge operation and finally the three-phase operation. However, to facilitate the explanation, the inverter mode of operation is discussed before the rectifier mode of operation.

2.1.1 Single-Phase Half-Bridge Operation

2.1.1.1 Half-Bridge Inverter mode

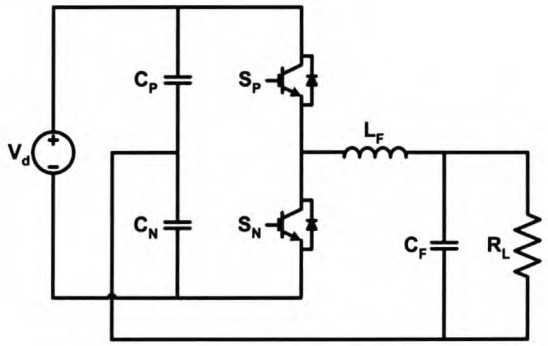


Figure 2-3: Half Bridge Inverter Structure

The single-phase half-bridge configuration, Figure 2-3 [68], is recognised by the return path of the load being connected to the centre point of the DC bus capacitors. With this type of converter, like most IGBT based converter configurations, bi-directional power flow can be performed. During inverting, the selected current convention is as follows: current flowing to the load, from the DC bus, is defined as positive current flow. Alternatively negative current flow implies current flowing in the other direction.

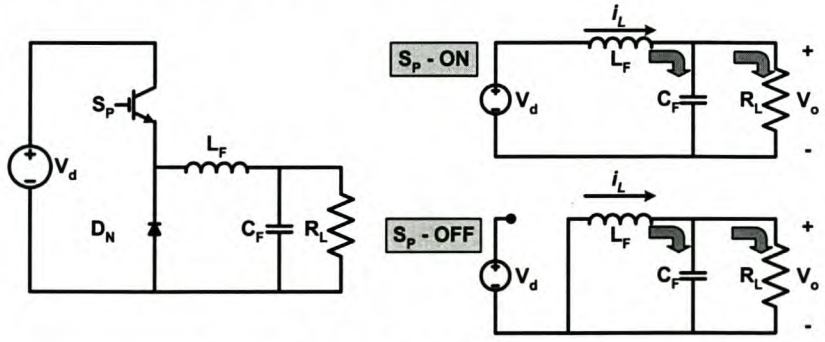


Figure 2-4: The Buck Converter Topology

The examination of a DC-DC buck converter, seen in Figure 2-4, facilitates the understanding of the half-bridge converter operation [68]. The two states a buck converter can be switched in are also shown in Figure 2-4. During S_P-ON, a DC voltage is applied to the inductor, capacitor and load, resulting in current flowing through the indicated paths. During S_P-OFF, the current stored in the inductor freewheels through diode D_N along the current paths indicated. The ratio of the output to input voltage for a buck converter is defined in (2.1), where V_o is the output DC voltage.

$$\frac{V_o}{V_d} = D = \frac{T_{on}}{T_s} \tag{2.1}$$

The ratio of ON time (T_{on}) for the switch S_P to the total switching period (T_s) is known as the duty ratio D, shown in (2.1). The OFF time, T_{off}, is typically $(1-D)$, or alternatively (T_s-T_{on}). In similar manner the half-bridge configuration makes use of a DC bus voltage, larger in magnitude than the required output voltage, to modulate an AC output waveform. The switches are controlled using various pulse width modulation (PWM) techniques, the simplest being open-loop sinusoidal bipolar PWM seen in Figure 2-5.

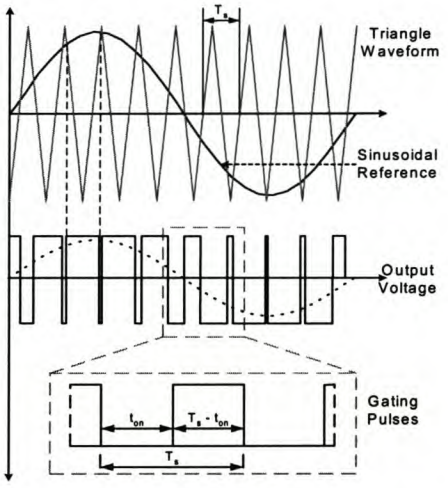


Figure 2-5: Bipolar Open-loop Sinusoidal PWM Technique

The converter is switched by alternately switching the switches S_P and S_N on and off. Examination of Figure 2-6(A) shows that while the S_P switch is ON, S_N is OFF. To achieve this, Figure 2-5 warrants closer examination. A sinusoidal reference waveform is compared with a triangular waveform that has a frequency equivalent to the desired switching frequency. When the sinusoidal reference is larger than the triangular waveform, the switch S_P, seen in Figure 2-6, is switched on and the voltage on the converter side of the inductor is $\frac{1}{2}V_d$. During this time the switch, S_N, is kept OFF. The opposite is also true for when the sinusoidal reference waveform is smaller than the triangular waveform. S_P is switched OFF and S_N is switched ON and the voltage on the converter side of the inductor is $-\frac{1}{2}V_d$. This is known as complementary switching. The resultant gating pulses, at the bottom of Figure 2-5, are sent to S_P and S_N.

It is the inductor, in Figure 2-6(A) and (B), that is responsible for the waveform modulation. By applying a square voltage waveform to the inductor, seen in Figure 2-6(C), a linear increase in current through the inductor occurs according to relationship (2.2).

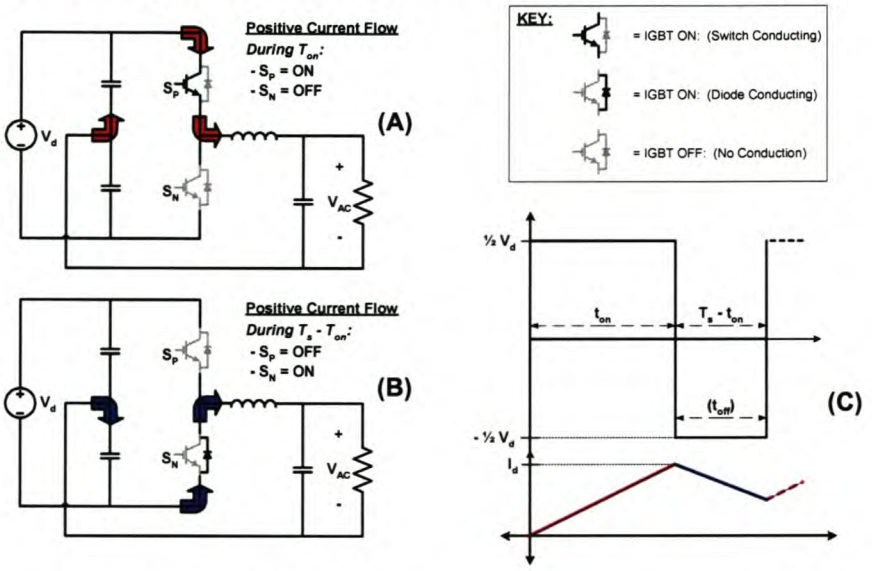


Figure 2-6: Half-Bridge Inverter Operation: (A) S_P ON, (B) S_P OFF, (C) Voltage & Current Output

In the case of the half-bridge inverter, the voltage magnitude, of equation (2.2), is the difference between ½V_d, the applied DC bus voltage, and the load counter Emf.

$$V = L\frac{di}{dt} \tag{2.2}$$

Examining Figure 2-6(B), during T_{off} and positive current flow, it is seen that -½V_d is applied to the load. This occurs when the inductor forces the diode of S_N to become forward biased, resulting in the centre point voltage of the phase-arm dropping to -½V_d. The current decreases in a linear fashion, like that seen in Figure 2-6(C). The modulation of a sinusoidal load current through the inductor is achieved by varying the duty ratios of the switches, and subsequently the square wave output waveforms, in the same manner as in Figure 2-5.

2.1.1.2 Half-Bridge Rectifier Mode

Half-bridge converters are, as previously mentioned, capable of bi-directional power flow. The half-bridge topology is capable of rectifying an AC source into a DC value, larger in magnitude, using a technique known as active rectification. A control technique is used to regulate the magnitude of the DC bus voltage and subsequent removal of the harmonics associated with passive rectification is also achieved. The active rectifying mode of operation for a half-bridge converter is derived from the standard boost converter, seen in Figure 2-7 [68].

During the time when switch S_N is ON, current flows through the inductor L_F, storing energy in the inductor, while at the same time the load current is sourced from the capacitor C_F. When S_N is switched off, the stored energy in the inductor flows through the load and the capacitor, resulting in the capacitor being charged, or boosted, and the DC load voltage, V_o, hav-

ing a magnitude larger than that of the supply voltage.

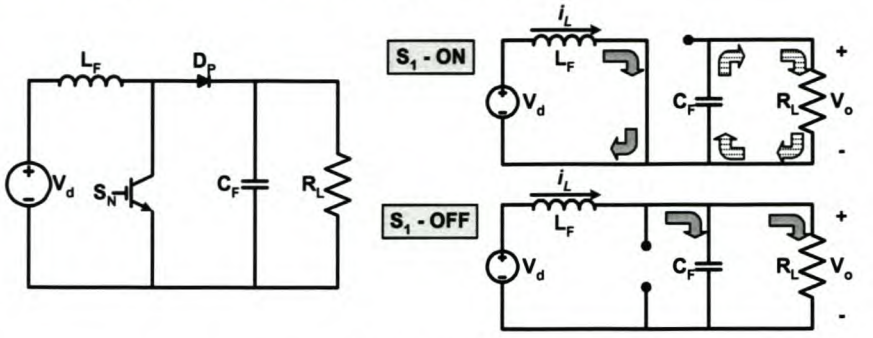


Figure 2-7: The Boost Converter Topology

The ratio of V_o to V_d for a boost converter is seen in (2.3).

$$\frac{V_o}{V_d} = \frac{1}{1-D} \tag{2.3}$$

This principle, applied to converter configuration, enables active rectification and bi-directional power flow. Figure 2-8 illustrates the half-bridge topology rectifier operation [15][71]. During rectification, positive current is defined as the current flowing into the DC bus, unlike the inverter mode convention of Figure 2-6. Active rectification also requires the DC bus voltage to be larger than the maximum peak AC voltage. A DC link voltage lower than the peak voltage would result in the anti-parallel, or freewheeling diodes, conducting and resulting in passive rectifying.

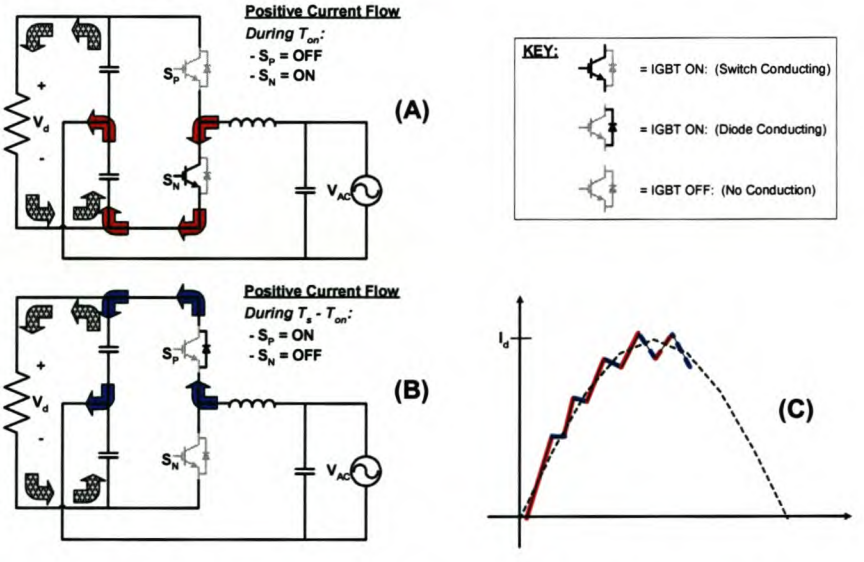


Figure 2-8: Half-Bridge Rectifier Operation: (A) S_P OFF, (B) S_P ON, (C) Sinusoidal Current Drawn from Source

Active rectifying uses the inductor as an energy storage device to force current to flow into the DC bus. To achieve this the bottom switch S_N is closed first, Figure 2-8(A), while the AC voltage source increases sinusoidally. This results in a negative voltage being applied to the switch side of the inductor. With an increasing positive AC voltage applied to the inductor, a sharp positively rising current slope in the inductor occurs. At the same time, and conse-

quently only for the half-bridge configuration, this current charges the bottom capacitor. The next switch operation, Figure 2-8(B), S_P - ON and S_N - OFF, results in the inductor current freewheeling through the diode of S_P. The voltage applied to the switch side of the inductor is positive and larger than the AC voltage, and results in the negative slope of the decreasing inductor current, Figure 2-8(C). During this switch state, the freewheeling current charges the top capacitor, a characteristic unique to the half-bridge topology resulting in voltage doubling [71].

Using the bipolar switching technique, the switched current into the DC bus can be sinusoidally modulated, resulting in DC bus boosting and the supply having a lower harmonic content. While acceptable for explanation purposes, open-loop control is not used when actively rectifying. Control over the current being fed into the DC bus is required, since no control results in unpredictable current oscillations and unstable DC bus voltages being generated. The modulation of the current waveform is realised, in this case, by using the predictive current control loop [72], typically used for single-phase or de-coupled converters.

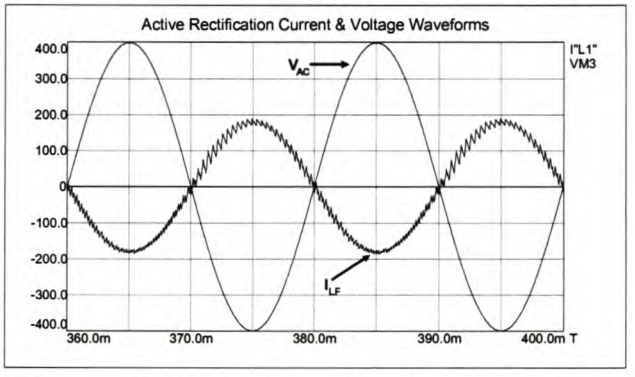


Figure 2-9: Typical Half-Bridge Converter Active Rectification Waveforms

Using predictive current control and the bipolar switching technique, sinusoidal active rectifier current and voltage waveforms are simulated and their results represented in Figure 2-9. Insight as to how the capacitors are charged is however obtained by examining Figure 2-10, the simulated DC side voltages and currents.

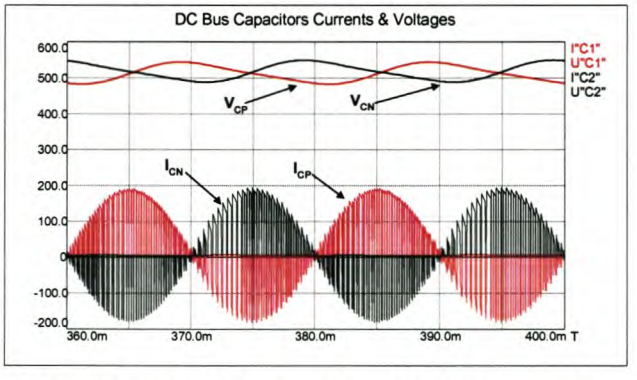


Figure 2-10: Typical Half-Bridge Active Rectifier DC Voltage and Current Waveforms

The DC bus voltages measured are on a per-capacitor basis, thus the total DC bus magnitude is in the order of 800 V, including a 100 Hz ripple component, the product of the two 50 Hz components present in both DC capacitor voltages. The DC current components charg-

ing the capacitors are also displayed, the 50 Hz component clearly being seen. The oscillation around the centre point occurs because the current through the capacitors changes direction.

2.1.2 Single-Phase Full-Bridge Operation

The full-bridge converter, seen in Figure 2-11, is an extension of the half-bridge topology, and makes use of an extra phase-arm. The connection between the load and the centre point of the capacitors is also not present in this topology [68].

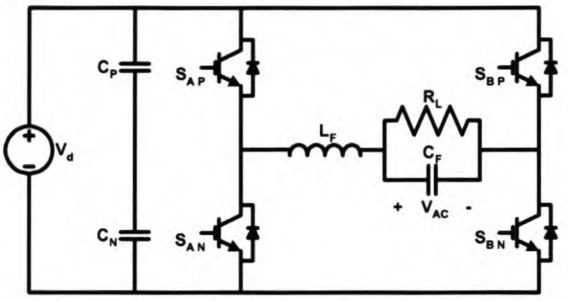


Figure 2-11: Single-Phase Full-Bridge Converter

2.1.2.1 Full-Bridge Inverter Mode

During inverting mode, the full-bridge topology subjects the load to double the output voltage, whilst operating at the same DC bus voltage levels as the half-bridge topology. Operation, using the bipolar switching technique, can be seen in Figure 2-12.

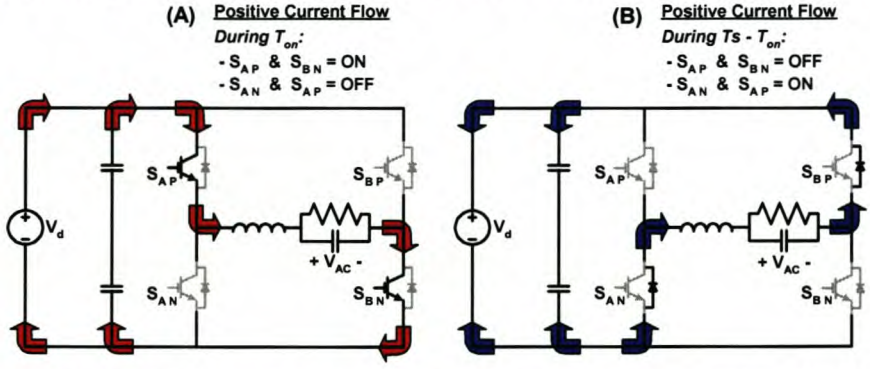


Figure 2-12: Full-Bridge Operation. (A) Positive Current Flow. (B) Freewheeling State

The main benefit obtained using this topology is the reduced current requirements of the switches when switching the same power levels as that of the half-bridge topology. With the load being subjected to double the driving voltage, the required current is halved, while supplying the same power. The half-bridge topology would require the switches to be double the current rating for the same power levels.

A further benefit is realised when analysing the three possible switching states available to the full-bridge converter, seen in Figure 2-13. Ignoring the counter Emf, the positive and negative states are obtained by changing the polarity of the DC applied to the load, seen in Figure 2-13(A) and (C). It is specifically the zero state, Figure 2-13(B), that allows for more advanced controlling of the converter.

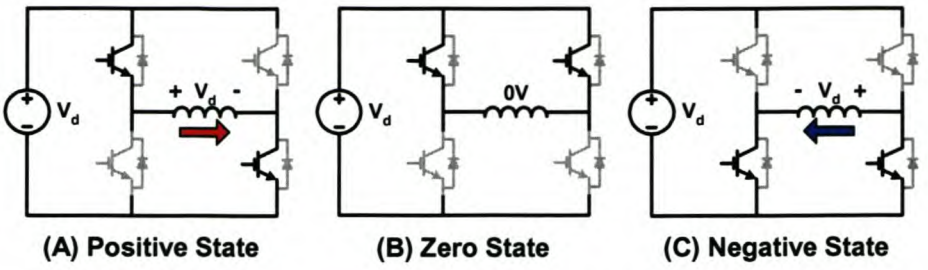


Figure 2-13: Three Converter States of a Full-Bridge Single-Phase Converter

This state, obtained by connecting the load completely to either the positive or negative DC bus rails, ensures that there is no differential voltage over the load, and subsequently no current flows.

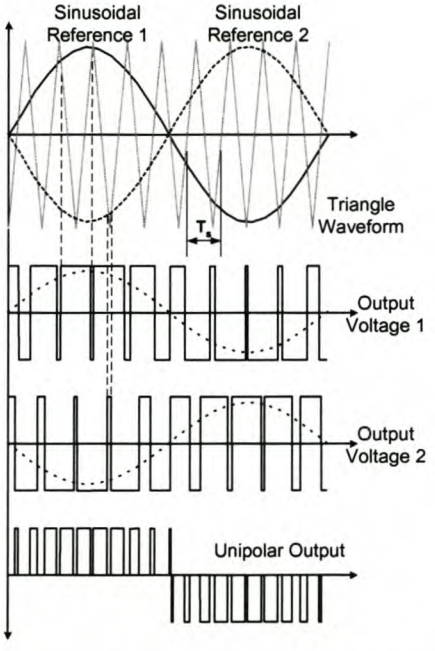


Figure 2-14: The Unipolar Open-loop Switching Technique

With the aid of the zero state it is possible to independently control each of the phase-arms, using a technique called unipolar switching, illustrated in Figure 2-14. This technique uses two individual sinusoidal reference waveforms, displaced from each other by 180°, each generating the gating pulses for an individual phase-arm. With both phase-arms switching independently, and the zero states being switched, the resultant driving voltage over the load takes the form of the unipolar output voltage waveform seen in Figure 2-14. The gain is an output voltage with double the original switching frequency. The advantage of this is that the switching harmonics shift to a higher frequency, appearing as sidebands of twice the apparent switching frequency [70]. The disadvantage is that the switching losses also increase because of the higher apparent switching frequency.

2.1.2.2 Full-Bridge Rectifier Mode

During full-bridge rectification the positive current convention is once again denoted as flowing into the DC bus, observed in Figure 2-15. Using bipolar switching, Figure 2-5, dur-

ing the time T_{on}, the current flows in the direction seen in Figure 2-15(A), through the DC bus capacitors. During freewheeling, the period T_s-T_{on}, the current flows in the opposite direction, Figure 2-15(B), through the DC bus capacitors.

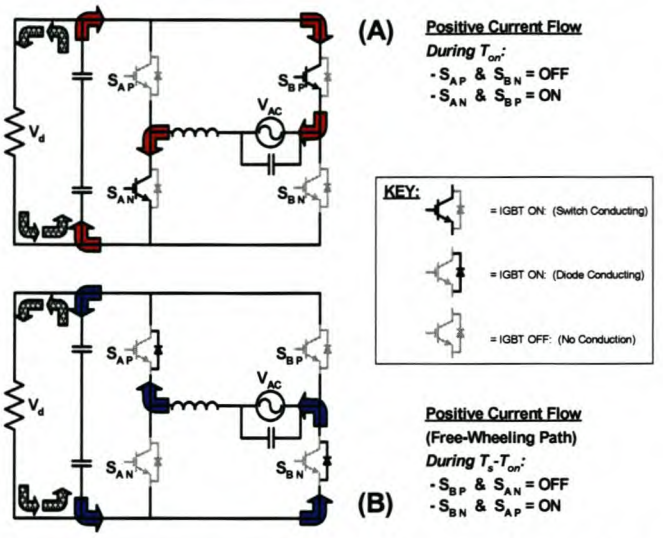


Figure 2-15: Full-Bridge Rectifier Operation. (A) During T_{on}, (B) During T_s-T_{on}

The relationship between ON time and freewheeling time dictates the magnitude of the DC bus charging, remembering that the DC bus value needs to be larger than the AC source voltage to prevent passive rectification. The primary difference between the full-bridge and half-bridge topologies is that the full-bridge is not a doubling circuit, i.e. the peak-to-peak voltage is applied to the full DC bus capacitors when charging, and not half of the DC bus capacitors, as is the case in the half-bridge topology.

Similar to the half-bridge converter, the open-loop principle serves as a good tool in the explanation of operation; however, practical realisation of this still requires a current controller. Using predictive current control [72] and bipolar switching, the source voltage and current waveforms are simulated and shown in Figure 2-16.

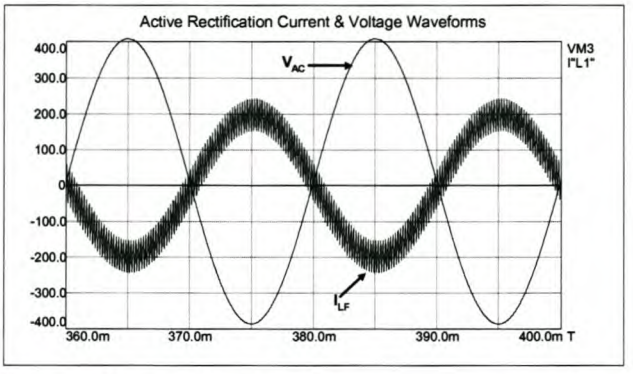


Figure 2-16: Typical Full-Bridge Converter Active Rectification Waveforms

It is evident from the inductor current waveform that the ripple component is larger than that simulated in the half-bridge topology. This is because the DC bus side of the inductor is swung between the DC values V_d and $-V_d$, in the period between conduction and freewheeling, resulting in higher ripple, while the half-bridge converter utilises only half of the DC bus

value.

Figure 2-17 shows the simulated DC bus capacitor voltage and current waveforms, while actively rectifying using a full-bridge converter. The 100 Hz voltage ripple component is again present and is a result of the current flowing through the capacitors, also shown in the figure. The variance between the half-bridge and full-bridge topologies is seen in the DC current waveforms.

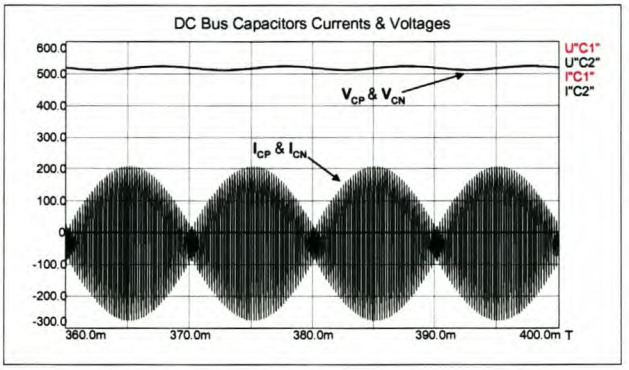


Figure 2-17: Typical Full-Bridge Active Rectifier DC Voltage and Current Waveforms

The full-bridge converter current flows through both DC bus capacitors at all times, unlike the half-bridge, using the centre point connection, causing the current to flow alternatively through capacitors C_P and C_N, Figure 2-10.

For the half-bridge and full-bridge simulations the physical DC bus voltage magnitudes are the sum of the two capacitor voltages measured. The capacitor voltage waveforms of the full-bridge also require examination, as the full-bridge converter is not a doubler circuit, and the magnitudes are similar. This is because a current controller used the same reference values and AC side voltages, thus resulting in identical power levels being pumped into the DC bus, hence the similar DC bus voltage magnitudes.

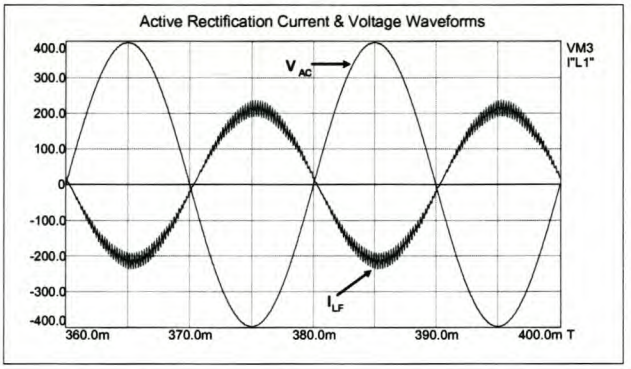


Figure 2-18: Full-Bridge Converter Active Rectification Waveforms using Unipolar Switching

The rectifier current waveforms of a full-bridge converter using unipolar switching and a predictive current controller [72] are simulated and seen in Figure 2-18. The unipolar technique has a switched current with a lower ripple and the effective doubling of the switching frequency, as discussed.

The DC side waveforms, during unipolar switching, are represented in Figure 2-19. The DC capacitor voltages are identical with the 100 Hz ripple present and when summed equal

approximately 1100 V.

Interesting to note are the DC capacitor currents during unipolar switching. The DC capacitors are exposed to a one-directional current only, a result of the switching technique.

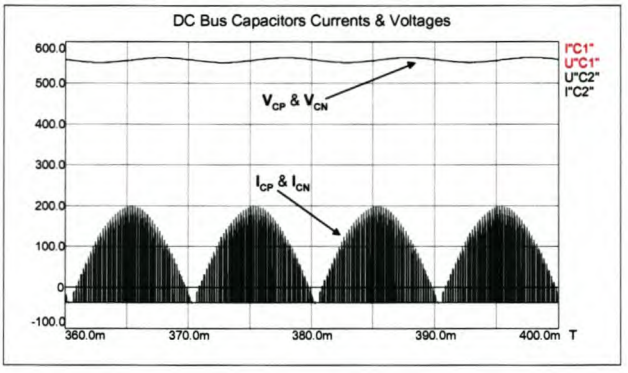


Figure 2-19: Unipolar Switched Full-Bridge Active Rectifier DC Voltage & Current Waveforms

During purely inverting mode, all the capacitor currents flow in the opposite direction to that observed during rectifying mode.

2.1.3 Three-Phase Converter Operation

Three-phase converters are essentially extensions of the half-bridge and full-bridge single-phase converters, obtained by the addition of extra phase-arms. Three-phase converters can be classified into two configurations. The first is the de-coupled converter configuration shown in Figure 2-20, and the second is the three-phase coupled configuration seen in Figure 2-21. The de-coupled converter configuration is essentially three single-phase half-bridge converters placed in parallel.

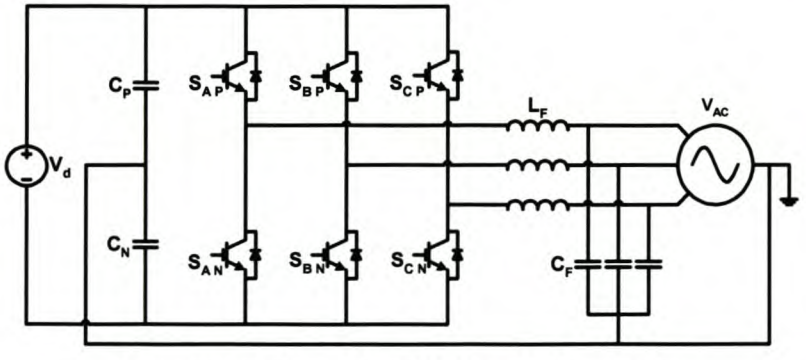


Figure 2-20: Three-Phase De-Coupled Converter

The neutral connection from the star point of the load to the centre point of the DC bus prevents waveform modulation in one phase-arm from affecting the waveforms modulated in the other two phase-arms. A load imbalance results in a neutral current flowing, which in turn returns through the centre point of the DC bus capacitors, instead of back through the other phase-arms.

On the three-phase coupled converter, seen in Figure 2-21, there is no connection between the centre point and the star point of the load, typical of a motor load configuration. For the coupled converter the only return path for load imbalance current is through the adjacent

phase-arms, affecting their output waveforms, hence the coupling effect. This problem is typically overcome by using the space vector switching technique, where the coupled three-phase waveforms are generated, by making use of a reference that is generated in a two-phase de-coupled plane.

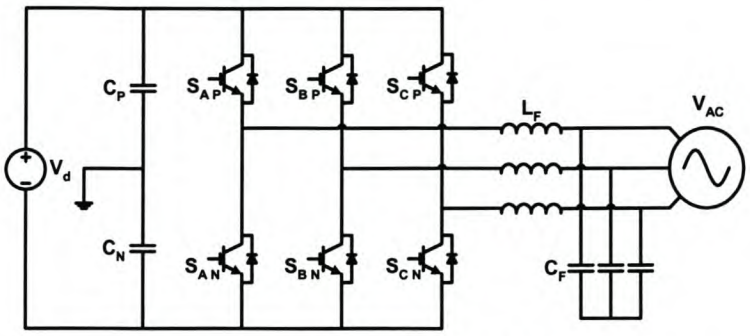


Figure 2-21: Three-Phase Coupled Converter

This technique is thoroughly discussed later in this thesis.

2.1.3.1 Three-Phase Inverter Mode

Using the inverting principles applied to both of the single-phase converter modes, the inverting mode of operation for the three-phase converter is simulated and represented in Figure 2-22. The three-phase inverting currents are exactly in phase with their respective voltages, and can be used to supply a variety of three-phase loads.

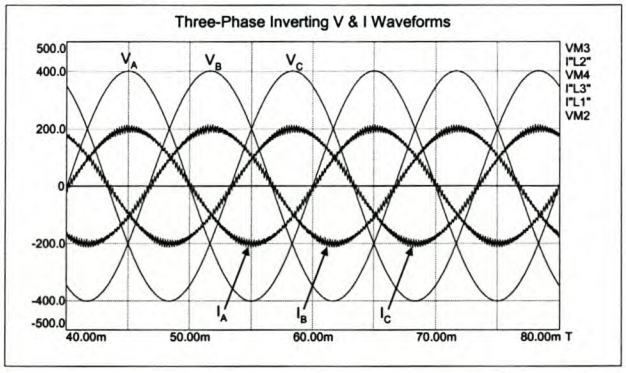


Figure 2-22: Simulated Three-Phase Converter Inverting Waveforms

2.1.3.2 Three-Phase Rectifier Mode

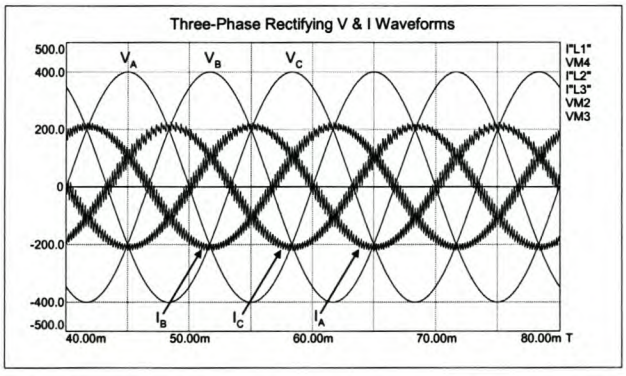


Figure 2-23: Simulated Three-Phase Converter Rectifying Waveforms

A simulation of the rectifier mode for a three-phase converter is shown in Figure 2-23. The difference between this and the previous mode of operation is that the current flows in exactly the opposite direction, as is expected of an active rectifier. This type of operation is particularly beneficial when supplying a DC load from a three-phase source, and results in a low amount of current harmonic being generated.

2.2 Chapter Summary

Having discussed the various modes of operation for the IGBT based converters, insight is gained into how the converter units perform the inversion and rectification functions. The simulated examples of their bi-directional power flow capabilities provide insight into their ability to regulate currents with a wide variety of wave shapes and phase shifts. It is this dynamic ability that makes them ideally suited to perform the functions required by the traction and MVDC applications. The extent of their ability is dealt with in the next chapter.

Chapter 3 Converter Requirements

In Chapter 1 the thesis objectives indicated that two specific multilevel topologies are to be investigated, with regard to their practical performance, as potential candidates for traction and MVDC applications. Chapter 1 also indicated the benefits of further enhancing the applications, thereby increasing the application functionality. This chapter does not deal with the multilevel converter topologies, neither their performance. It does, however, focus on the application requirements associated with enhancing their performance. In order to suggest a topology with the appropriate performance capabilities, a thorough understanding of the power network conditions, associated traction and MVDC applications is required.

This chapter identifies system configurations and power network compensation concepts. This is done to determine what roles are required to be performed by compensating devices, be they static or dynamic. Focus is placed on how these functions are traditionally performed. The impact on power quality and the limitations of these devices are discussed. Finally the specific tasks performed by the traditional compensation are re-evaluated using IGBT based technology. The added functional performance of converters whilst being applied in MVDC and traction applications is also discussed.

3.1 Required System Configurations

The typical connections of network modifiers, currently used in power systems, are seen in Figure 3-1. The series and shunt connections are ultimately the two basic connection strategies, whereas the third, the series-shunt connection, is the combination of the two.

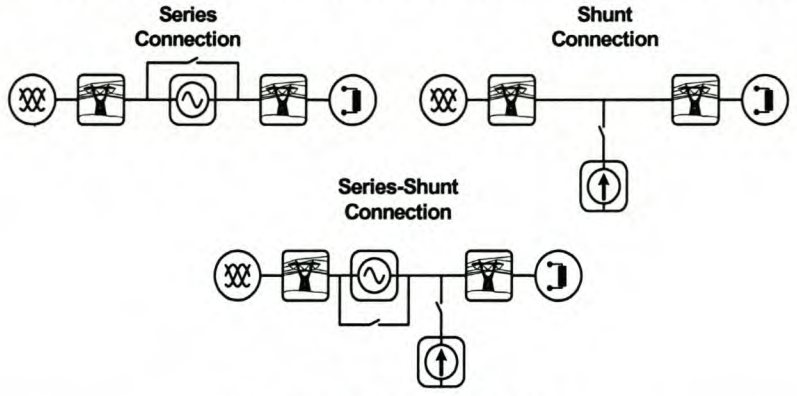


Figure 3-1: Connection Configurations

Series connected devices enable the improvement of the voltage waveform on the system, be it by the reduction of line losses or by inserting a compensating voltage to modify the receiving end voltage. Shunt connection allows for the injection into or absorption of current from the network. This implies power, real or reactive, modification to the power network. Series-shunt connections make both the series and shunt functions available to the device.

Figure 3-2 is a visual representation of the various compensating requirements on the power network, when considering the traction and MVDC applications. Each requirement is

discussed separately in the following sections, as well as the existing network solutions that are widely used.

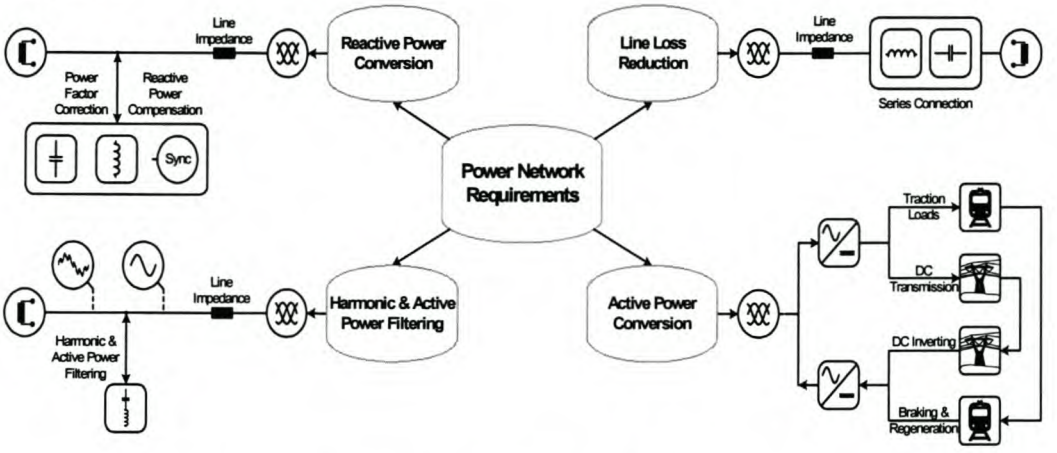


Figure 3-2: Compensating Concepts

3.2 Traditional Fixed and Dynamic Solutions

3.2.1 Active Power Conversion

Various applications require real power to be converted from one form to another, typically AC to DC and vice versa. This section deals with the bi-directional power flow requirements and the traditional techniques used to obtain this bi-directionality. Originally power flow between AC and DC voltage sources was only possible using a DC machine coupled to a synchronous machine via a mechanical link, like that seen in Figure 3-3. The mechanical connection enabled AC power to be generated while the DC machine acted as the prime mover. Alternatively DC power could be generated while the synchronous machine acted as the prime mover.

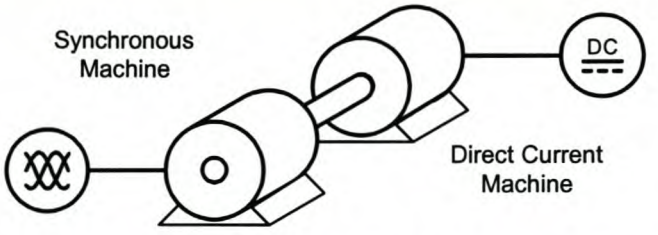


Figure 3-3: AC Synchronous Machine and DC Machine Combination

This method of AC-DC or DC-AC conversion has been widely used in the past; however, the mechanical nature of the machines results in high maintenance costs due to their moving parts.

3.2.1.1 AC-DC Power Conversion - Static and Dynamic

Technological advances led to high power diodes being developed as a cheap and efficient solution for converting AC to DC power, like the typical full-bridge rectifier seen in Figure 3-4. Existing traction applications in South Africa extensively make use of an extension of the

single-phase full-bridge passive diode rectifier [68] in Figure 3-4, namely the six and twelve pulse three-phase rectifiers.

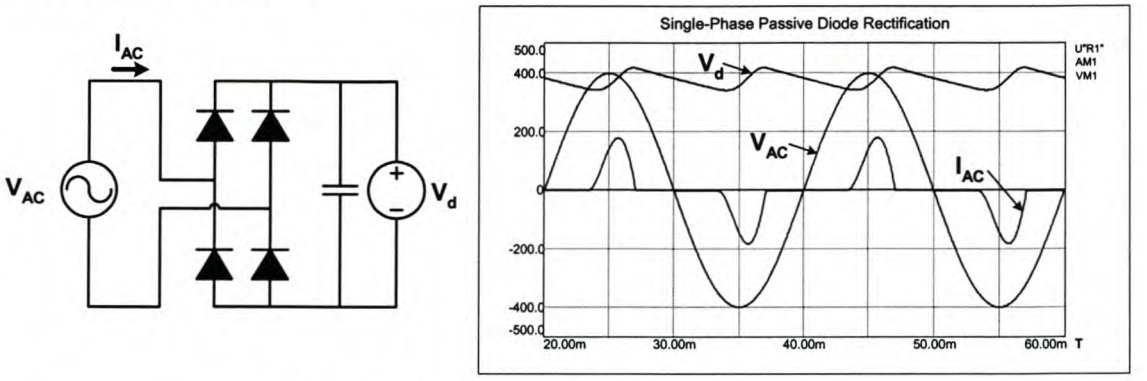


Figure 3-4: Passive Diode Rectifier Operation

The diode rectifier and simulated waveforms in Figure 3-4 show that the magnitude of the rectified DC bus voltage is dependent on the size of the AC input voltage waveform. Since the AC voltage magnitudes are fixed, there is no control over the DC magnitude. Furthermore bi-directional power flow is not possible as the diodes can only conduct in one direction. Passive rectifying also results in harmonics being generated on the supply side, due to the non-sinusoidal current conducted by the diodes, observed in Figure 3-4. This occurs when the diodes are forward-biased and conduct when the anode voltage exceeds the DC link voltage.

The ability to perform high voltage bi-directional power flow and DC bus regulation using silicon devices was first realised using back-to-back thyristor bridges like those seen in Figure 3-5.

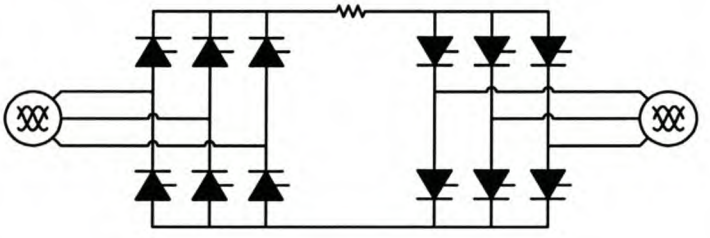


Figure 3-5: Thyristor Based HVDC Link

A prime example of high voltage direct current (HVDC) power transmission, the thyristor bridges modify the power by rectifying AC into DC and inverting DC into AC, using the AC system voltages to commutate the thyristors. The functional benefits are made apparent when transporting high power over large distances. AC line losses are removed and networks operating at different system frequencies can be connected. During the rectifying mode, a mode also used on traction systems, the thyristor operation is best explained while supplying as resistive DC load, as seen in Figure 3-6. The simulated waveforms show the relevant AC and DC side waveforms. During rectifying, Figure 3-6, the thyristor gating pulses are fired at angles between 0°and 90°, resulting in the DC voltage component shown.

Variation of the gating angle results in a variation in the magnitude of the DC side voltage, a function of the average conduction time.

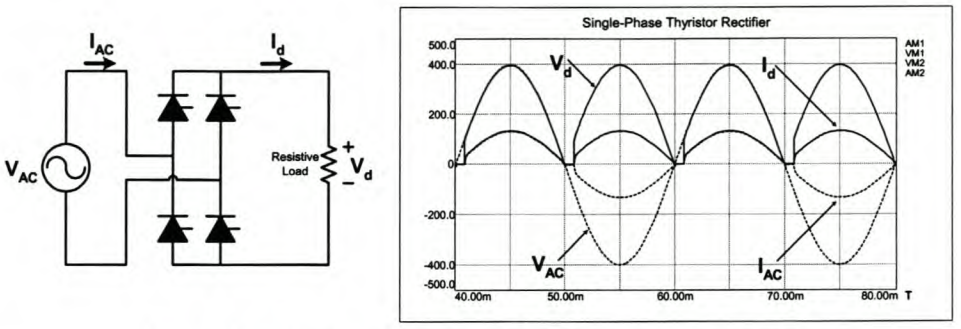


Figure 3-6: Thyristor Rectifier Operation (Resistive Load)

The closer to 0° the firing angle is, the larger the magnitude, while an angle close to 90° results in a low average DC bus voltage [68]. However, since most HVDC applications make use of an inductive component for smoothing, the DC side voltages usually take the form of those displayed in Figure 3-7. The simulation model is that of a thyristor rectifier supplying a current source load. It shows the typical commutation expected when inductive elements are involved.

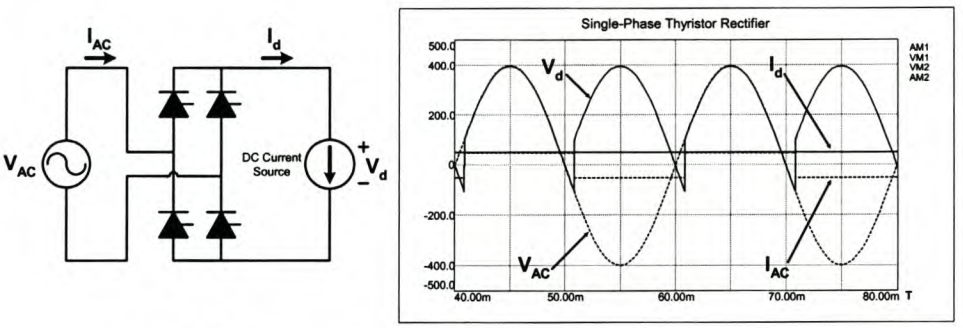


Figure 3-7: Thyristor Rectifier Operation (Current Source Load)

In Figure 3-7 the same gating pulses are used as in Figure 3-6. The result is an average DC voltage that is positive, as before, while the AC side current supplying the load is a square wave, which in turn results in current source type harmonics.

3.2.1.2 DC-AC Power Conversion - Dynamic

Figure 3-7 provides insight into operational behaviour of the thyristor bridge operation as an inverter. Thyristor inversion is simulated in Figure 3-8. Changing the firing angle of the thyristors to gate between 90° and 180° results in a line commutated DC bus voltage with a negative average value [68].

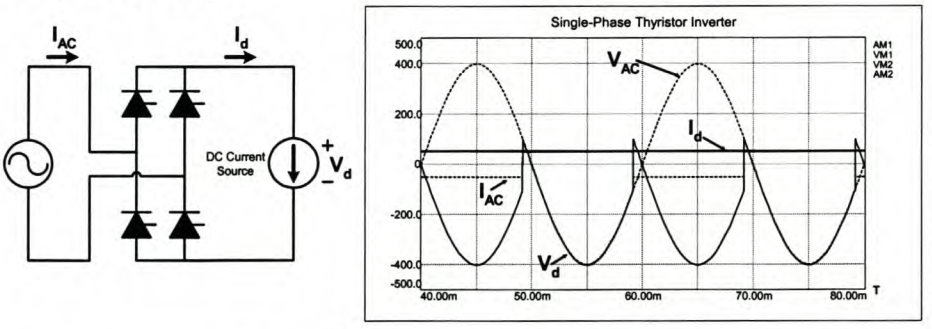


Figure 3-8: Thyristor Inverter Operation

These negative DC voltages in conjunction with the positive DC current result in negative power flow, i.e. flowing from the DC side to the AC side. This technique is currently widely used in HVDC applications; however, the line commutated switching nature of the thyristors leads to a high level of harmonic pollution. From the examination of the thyristor operation it can be concluded that an alternative solution that provides higher efficiency and produces less harmonics is preferable.

One major limitation is that of the cost of these HVDC links. They are only economically justifiable when operating at very high power ratings. It is for this reason that the HVDC lines operate at typical line voltages of 800 kV. The key is to be able to perform this functionality at lower voltage ratings, i.e. lower power, and still make the device financially affordable.

3.2.2 Line Loss Reduction - Static Series Compensation

Referring back to Figure 3-2, line loss reduction is dealt with next because this type of static in-line series compensation forms the basis for the subsequent compensation sections. In all power networks, the series impedance of the line feeding the load results in a voltage drop over that line. These impedances usually comprise a resistive and inductive component, as seen in Figure 3-9(A), of which the inductive component is usually dominant.

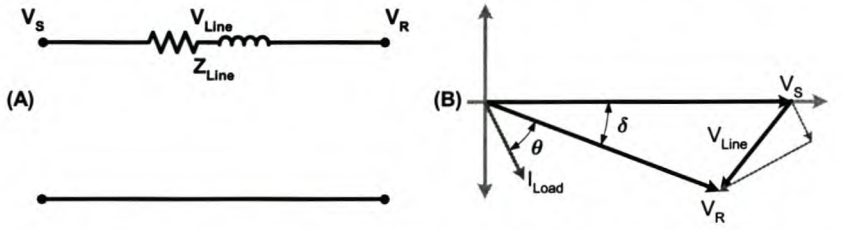


Figure 3-9: Effect of Line Impedances on System Voltages

The line impedance and load current results in a voltage drop over the line. This voltage drop yields a receiving-end voltage, V_R, which is smaller in magnitude and displaced from the sending-end voltage, V_S, by an angle δ, known as the load angle, seen in Figure 3-9(B). The magnitude of the load angle depends on two factors, the largest factor being the size of the line inductance, with the second being the power factor of the load current, which has a very limited impact.

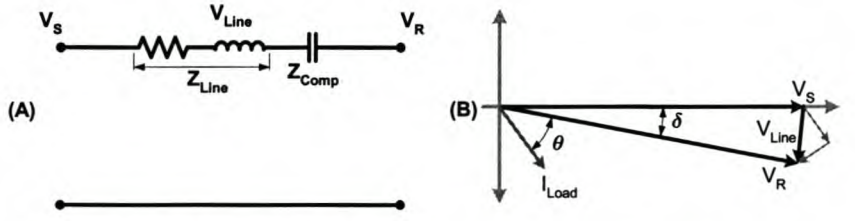


Figure 3-10: Effects of Static Series Compensation on System Voltages

By inserting a series capacitor in the line it is possible to reduce the inductive part of the series line impedance, seen in Figure 3-10(A). This action causes the load angle, δ, to reduce,

due to the smaller voltage drop over the line impedance, Figure 3-10(B). The net yield of this type of compensation is a rigid system with increased loadability. In essence these are exactly the conditions that motivate the use of MVDC, avoiding this line loss completely.

3.2.3 Reactive Power Conversion - Static Shunt Compensation

With the impact of the line impedance on a power network identified, it is necessary to identify the effect that the load power factor has. In Figure 3-11, the basics of static shunt compensation can be explained. Most loads are inductive, resulting in a lagging power factor on the load side. Large lagging or leading power factors are undesired because the utilities billing structures penalise consumers when their maximum demanded power exceeds their pre-determined power requirements.

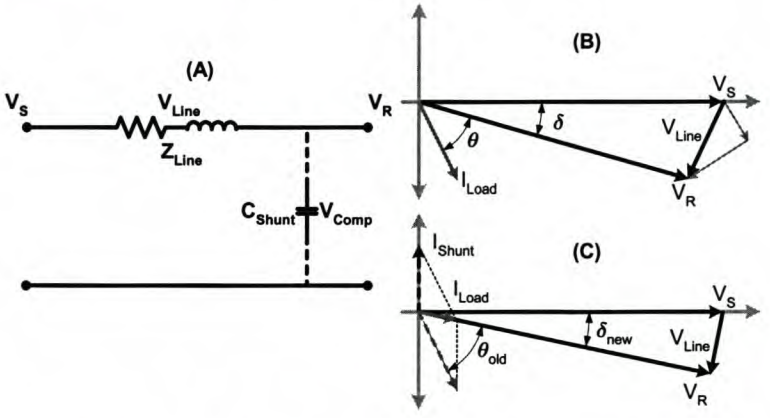


Figure 3-11: Static Compensation for the Voltage Drop Over a Line Supplying an Inductive Load. (A) The Single-Line Diagram. Vectors Before (B) & After (C) Shunt Compensation

Bad power factors cause the apparent power, S measured in VA, to be much larger than the real power consumed. Controlling of the power factor magnitude is dependent on the angle of the load current. In Figure 3-11(B) this angle is denoted as θ and it lags the voltage, V_R, due to the inductive nature of the load. By inserting a shunt capacitor in the circuit, drawing a 90° leading current, the inductive current drawn by the load is compensated for, improving the power factor as seen in Figure 3-11(C). In summary, shunt compensation improves the power factor, affects the magnitude of V_R and modifies the load angle to a very small degree, as seen in Figure 3-11(C). For practical purposes, shunt compensation is not used to modify the load angle, δ, because of its small compensating capability.

In Figure 3-12(A) to (C) a shunt inductor, drawing a 90° lagging current, is used to compensate for a leading load power factor. Leading power factors are commonly found on long point loads that are lightly loaded. Capacitive coupling between the line and ground occurs, known as the Ferranti effect. This effect does, however, decrease as the line is loaded more heavily. The large shunt capacitance results in the load having the large leading power factor, Figure 3-12(B), causing V_R to exceed the magnitude of V_S, potentially exceeding voltage insulation levels.

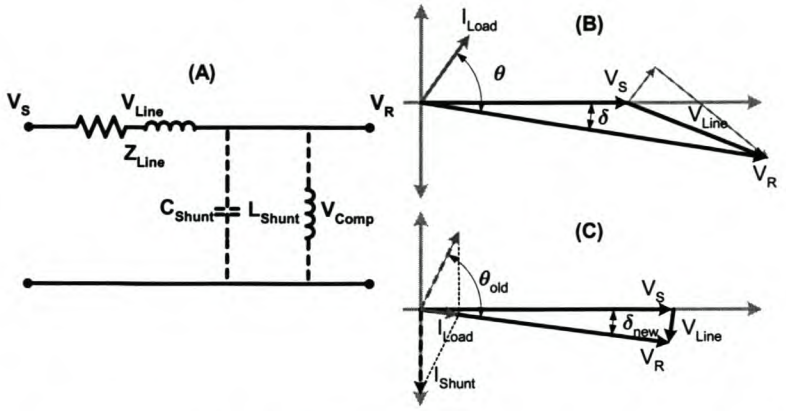


Figure 3-12: Static Compensation for the Voltage Drop Over a Line Supplying a Capacitive Load (A) The Single-Line Diagram. Vectors Before (B) & After (C) Shunt Compensation

Shunt reactive compensation, Figure 3-12(C), has the same effect as that seen in Figure 3-11, with the largest impact being the power factor and the size reduction of the load voltage V_R, seen in Figure 3-12(C). In conclusion, simple and inexpensive shunt compensation increases system efficiency; however, static shunt devices are prone to load variation and resonance, making them inefficient once again.

3.2.4 Harmonic and Active Power Filtering - Static Compensation

Another major concern is the generation of harmonics by non-linear loads on power networks. Seen as system pollution, it is responsible for increased losses and waveform deformation, and has increasingly become an area of concern. To ensure a high level of power quality and the mitigation of flicker, swell, impulse harmonics and phase unbalance [72], various devices and techniques are used to mitigate these harmonic components on power networks. Before the static compensation techniques are discussed, it is necessary to know what types of non-linear loads are responsible for the typical waveform distortions incurred on a power network. Numerous sources generate harmonics; however, the two most common types of sources are the current-source and voltage-source harmonics.

3.2.4.1 Current-Source Harmonic Sources

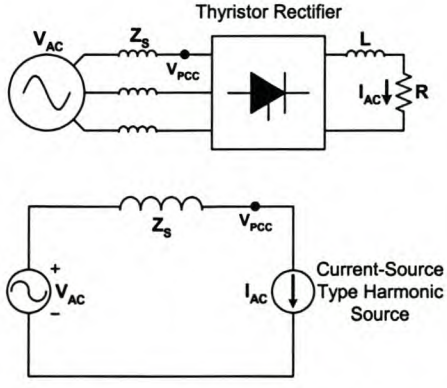


Figure 3-13: A Thyristor Rectifier and its Equivalent Circuit

The first type of harmonic source to be discussed is that of a non-linear load causing current-source harmonics, so classified because distortion primarily affects the current waveform of the supply. Typical non-linear loads that generate this type of harmonic are DC loads that employ the use of thyristor rectifiers, like that seen in Figure 3-13 [19][20][21].

Typical of the rectifier side of the traditional HVDC and traction applications, it is the switching operation of the thyristors in a rectifier that results in current harmonics being generated by the load. When using a three-phase thyristor rectifier, the supply side current waveforms distort like those seen in Figure 3-14.

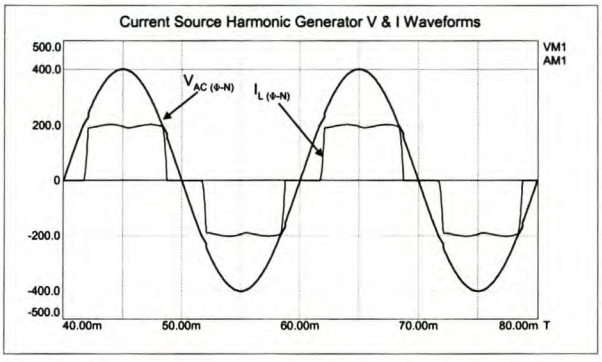


Figure 3-14: Typical Current Harmonics Generated when using a Thyristor Rectifier

The presence of the large DC inductance in the rectifier topology, used to ensure that a constant DC current is supplied to the load, needs to be considered. The high ratio of the load inductance to the source inductance [19], a condition typical to the thyristor rectifier, results in the non-linear harmonic current having little impact on the load voltage at the point of common coupling, V_{PCC}. The characteristic current drawn by the non-linear load, because of the large inductance (i.e. a small harmonic load), is less dependent on the AC side and thus the behaviour of the load is defined as a current source load [21][22]. It is for this reason that the rectifier and load are replaced by a current source in the equivalent circuit, seen in Figure 3-13. Ultimately, an ideal current-source harmonic source, generates harmonic currents dependent on the load, and is not affected by the source voltage.

3.2.4.2 Voltage-Source Harmonic Sources

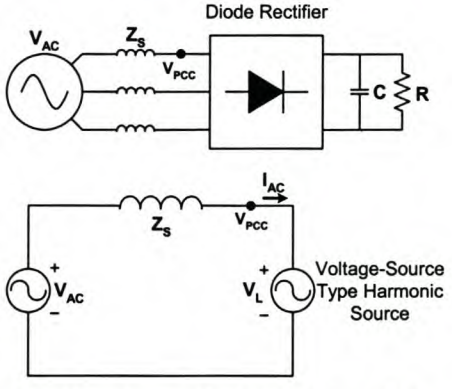


Figure 3-15: Passive Diode Rectifier and its Equivalent Circuit

The other type of harmonic source commonly found is the voltage-source harmonic source,

typically a passive diode rectifier that makes use of a capacitor on the DC side for smoothing of the DC ripple voltage, like that seen in Figure 3-15 [19][21]. Unlike the previous case, the voltage-source harmonic source has a small harmonic impedance (i.e. large harmonic load) when compared to the source impedance, Z_S.

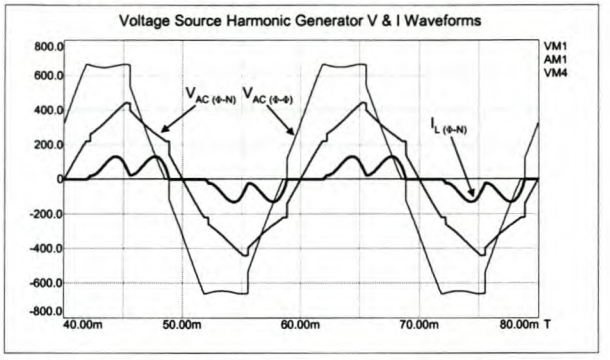


Figure 3-16: Typical Harmonic Waveforms Generated when using a Diode Rectifier

This implies that the harmonic current's magnitude on the DC side, seen in Figure 3-16, is greatly affected by the source impedance. Alternatively, the characteristic voltage waveforms, also seen in Figure 3-16, are less dependent on the AC side impedance of the rectifier, and thus the load behaves like a voltage source. The diode rectifier, using a smoothing capacitor, can thus be represented as a voltage source, seen in the equivalent circuit of Figure 3-15, and is defined as a voltage-source harmonic source. This also implies that the harmonic currents are dependent on the AC impedance as well as the characteristic harmonic voltage of the diode rectifier.

3.2.4.3 Static Harmonic Compensation Techniques

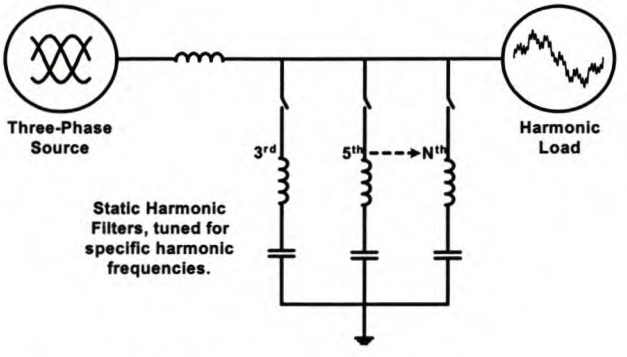


Figure 3-17: Tuned Harmonic Filters

Traditionally shunt passive filters have been used on power networks to mitigate the harmonics generated by the aforementioned harmonic sources. The filters consist of series connected inductors and capacitors connected in parallel to the power network, like those seen in Figure 3-17. Each filter is tuned to a specific harmonic frequency and is seen as a low impedance path for that specific harmonic current, thereby preventing the harmonic current from flowing to the source. They provide simple and inexpensive solutions, but have a number of serious disadvantages [19][20]. The first is that the source impedance strongly affects the per-

formance of the filter, since its filtering characteristics are theoretically determined by the impedance ratio of the source to the filter.

Another disadvantage is that the filter sinks harmonics from the source, and can go into series resonance with the source. Parallel resonance between the source and the filter can also occur, resulting in harmonic amplification, a highly undesirable condition. These serious disadvantages have led to the increased use of power electronic converters in the quest for harmonic mitigation, and will be discussed in the next section. These types of compensation techniques are widely used in the traction and HVDC applications

3.3 Active Power System Compensation

In Chapter 2, the operational capabilities of IGBT based converters were discussed. Applying converter based technology to the previously discussed power network requirements, the potential benefits can be evaluated. The combination of the inverting and rectifying modes, previously discussed, makes converter based technology an ideal solution for dynamic power compensation. In this section basic topologies used in power quality mitigation are discussed [16].

3.3.1 Series In-Line Devices

The in-line device consists of two back-to-back converters, connected via their DC buses, seen in Figure 3-18. Utilising the previously discussed inverting and rectifying modes makes the in-line topology an ideal solution for the mitigation of all waveforms that degrade the power quality.

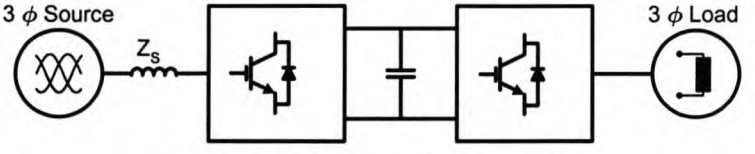


Figure 3-18: Series In-Line Device

The topology enables the total isolation of the load characteristics from the supply, via the DC link, while still enabling bi-directional power flow. It is functionally compared to the HVDC applications; however, operation will occur at reduced voltage levels, essentially MVDC. Case studies have been performed, and their results have shown that MVDC applications are more cost effective than traditional AC lines, where the distances are large [26].

Figure 3-19 is an example of this capability. The output stage is represented as a single-phase converter, for explanatory purposes. The output stage of the in-line device is capable of supplying the load and its harmonics, without it being seen on the supply side. Only real power is supplied from the input stage to the DC bus, while the load reactive power oscillates between the DC bus capacitors and the load. The input stage operates in the rectifier mode, drawing purely sinusoidal current that is in phase with the voltage. This also eliminates the problem encountered with static filters, namely that no source harmonics are absorbed by the

converter, eliminating the risk of series and parallel resonance.

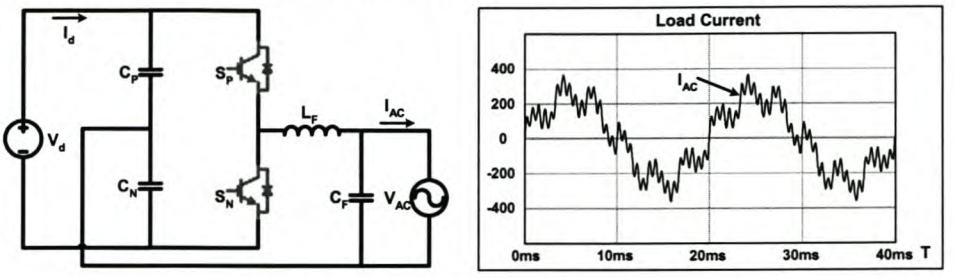


Figure 3-19: Non-Linear Load Compensation using In-Line Device

A further benefit of this in-line device is realised when overrating the input stage components, making it possible to perform shunt compensation, typically as explained in section 3.2.3. The simplest explanation for this technique of shunt compensation is understood by considering Figure 3-20, where the load is replaced by a voltage source.

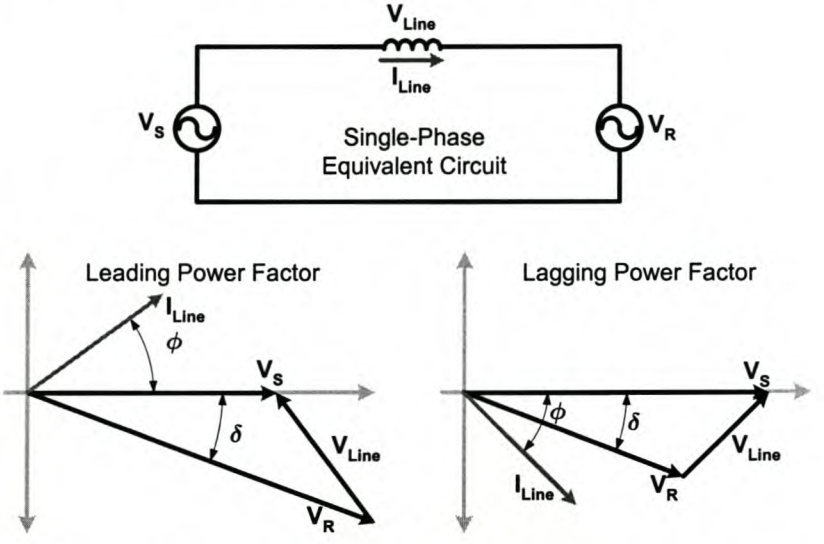


Figure 3-20: Power Factor Modification by Considering Two Voltage Source Model

By varying the angle of the load current, I_{Line}, being drawn from the source, it is possible change the magnitude of the voltage, V_R, on the receiving end of the line, thereby modifying the power factor of the load.

Examination of the active and reactive currents that the converter draws is required. A half-bridge single-phase converter's operation is simulated in Figure 3-21. The converter is controlled using a simple current regulator. In the simulation I_{Line}, the converter's modulated current, leads V_{PCC}, the voltage at the point of common coupling (PCC), by 90°. This results in the converter being seen as a shunt capacitor on the system. The versatility of converter based compensation is evident when considering that the magnitude and phase angle of the current can be varied. This makes it possible for the converter to make a smooth transition from a shunt inductor, when compensating for a lightly loaded long-line suffering from the Ferranti effect, and a shunt capacitor performing power factor correction for the same line as the loading increases.

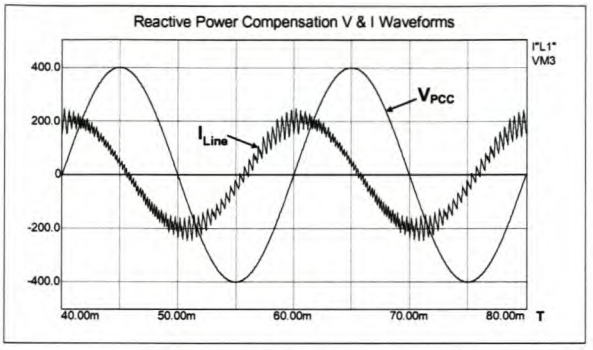


Figure 3-21: Simulated Converter Operation as a Shunt Compensator

To understand how the reactive power oscillates between the system and the converter, it is necessary to consider the simulated currents, flowing through the DC bus capacitors while switching the current, seen in Figure 3-22.

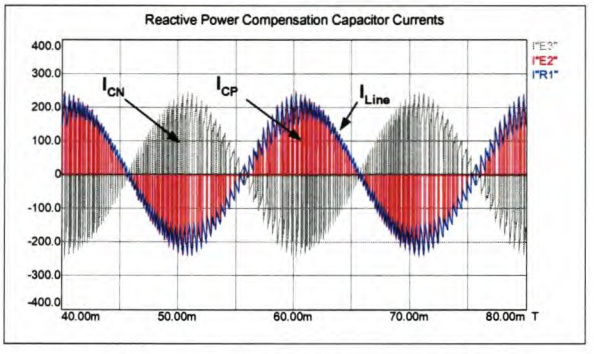


Figure 3-22: Simulated DC Bus Capacitor Currents during Shunt Compensation

The capacitor currents, in Figure 3-22, are represented on the same timescale as those in Figure 3-21, with I_{Line} superimposed on the DC capacitor currents. The phase angle of the capacitor currents shifts along with the reference current's phase angle. A current lagging the voltage by 90° will have the same effect with the capacitor currents shifting to lag the system voltage. When this type of compensation occurs, no power is removed from the DC bus. Although current is switched to compensate for the system during one fundamental period, the average power absorbed from the system is zero. The single-phase device also results in a 100 Hz voltage ripple on the DC bus, caused by the reactive power oscillation with the system. For a three-phase system, a 300 Hz ripple will be measured. Thus, with overrated switches, it is possible to actively rectify and perform shunt compensation and harmonic filtering.

In conclusion, the in-line device, performing all the required tasks of the MVDC functionality, has excellent power quality mitigating capabilities. However, the disadvantage is that the components have to be rated for the levels of compensation required and the active power transfer requirements. This is a large downfall of the topology, because most power system applications already require large ratings. Furthermore, two converters are required and this, in conjunction with the overrating of the components, increases overall converter cost, a major consideration when dealing with high power applications.

Alternatively, one converter unit can be used in a traction application. This type of con-

figuration converts AC into DC, using active rectification, ensuring a low level of electrical pollution on the power network. Further benefits are the regenerative capability. Currently on the South African railway network, the energy generated by the DC motors of electric trains during braking is dissipated into resistor banks. Using the single converter unit, and exploiting its bi-directional power flow capabilities, this energy can be injected back into the power network by inverting the DC.

3.3.1.1 Active Shunt Compensation

Active shunt compensation is an alternative solution that provides active power filtering with a considerable reduction in components, a function typically required by existing traction substations. Active shunt compensators consists of a single converter, connected in parallel with the power system, usually via a transformer, like that seen in Figure 3-23. In this configuration the converter is able to perform not only the harmonic filtering capabilities, but classical shunt compensation as well. The shunt connection allows for identical performance to that discussed in the in-line device, specifically the front-end reactive power compensation. A basic explanation for shunt compensation and its preferred mode of operation is best illustrated considering Figure 3-24. Being able to regulate a current with a varying phase angle facilitates the compensation for non-linear loads, be they periodic or aperiodic, typically expected with arc-furnace loads.

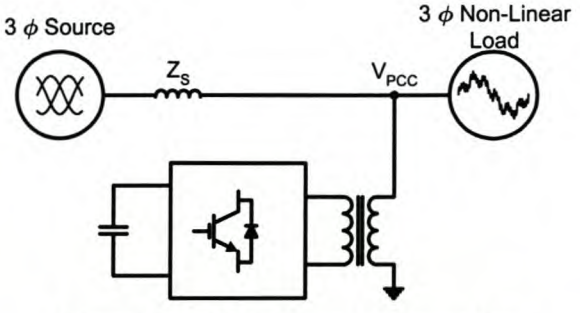


Figure 3-23: Active Shunt Compensator

Active filters thus have the added benefit of being able to perform harmonic cancellation and reactive shunt compensation. A shunt compensator is represented as a current source in its equivalent circuit, Figure 3-24. Noticeable in the figure is that the Norton equivalent circuit represents the load of a current source harmonic load. The reason for this is that, according to the publications [21] and [22], shunt active filters are best suited for current-source harmonic loads. The circuit equations in [21] show that the shunt compensator's performance characteristics are not influenced by the source impedance, Z_S, and are thus superior to static compensators, i.e. shunt harmonic filters, so long as the load harmonic impedance, Z_L, is much larger than the source's harmonic impedance. This condition is typically satisfied when supplying a current harmonic load, typically thyristor rectifiers. However, care needs to be taken when applying additional static compensators and shunt power factor correction capacitor banks in parallel to the compensator, as this will modify the harmonic impedance relation-

ship, more specifically Z_L.

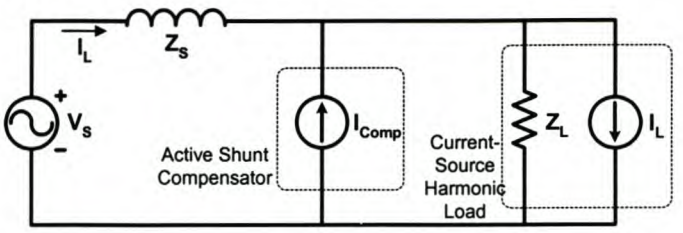


Figure 3-24: Shunt Compensator Equivalent Circuit

Further circuit equations in [21] show that, in trying to compensate for voltage harmonic sources, the shunt compensator compounds the harmonic distortion. This results in an increase in the harmonic currents.

The desired capabilities of shunt compensators are that they should compensate for both reactive and harmonic components. Ultimately they should compensate for all components that do not form part of the real power consumed by the load, actively filtering out all non-active power, giving rise to the term "Active Power Filters". Currently there are a few theories on the performance requirements of active power filters [16][17][18], derived from the definitions characterising non-active power. One suggestion is that during APF mode, the converter should ensure that the current drawn by the load is sinusoidal and in phase with the system voltage [17]. This technique ensures that the load generates low EMI; however, this technique also assumes the supply voltage is sinusoidal, a condition which may not be desired for the load. An alternative approach is to determine what the resistive components of the load are, i.e. components drawing real power, and to compensate for all other components [18]. This is achieved using various separation techniques, most of which are advancements on the theory proposed by Fryze in 1931 [18]. His theory has been widely expanded upon, but ultimately, as suggested by Peng in [18], the aim when performing the APF role is to compensate for all non-active components, without consuming or contributing any real active power, over a fundamental period. This technique is best realised by considering (3.1). G is the conductance, P the power and u the instantaneous RMS voltage.

$$G = R^{-1} = \frac{P}{u^2} \tag{3.1}$$

$$i_a = G \times u \tag{3.2}$$

From (3.2) it is possible to obtain i_a, the active portion of the current supplied to the load, i, seen in (3.3). Knowing the active current component of the load current enables compensation for the non-active components to be performed.

$$i_n = i - i_a \tag{3.3}$$

The shunt-connected converter supplies the non-active current, i_n, by means of current control, discussed earlier.

In conclusion, shunt active filters are far superior to static shunt compensators, and are less sensitive to source impedance variations, provided that the source load harmonic impedance

ratio is not significantly altered on the load side. They are ideally suited to current-source harmonic cancellation, but not voltage-source harmonic cancellation.

In traction applications this type of connection can extend the operational capabilities of the converter even further. Connecting the converter in parallel with the existing thyristor rectifiers, it is possible to supply the DC bus with the traction DC voltage. The device is thus able to perform shunt active power filtering on the power system being polluted by the thyristor rectifiers. It is also possible to perform power regeneration using this connection strategy, further extending the converter functionality.

3.3.1.2 Active Series Compensation

Active series compensation is realised by inserting a dynamic compensating voltage in series with the power network. A converter, with a configuration identical to the converter used for shunt compensation, is connected in-line with the power network using an injection transformer, like that seen in Figure 3-25. This form of compensation competes with the static in-line compensation discussed in 3.2.2.

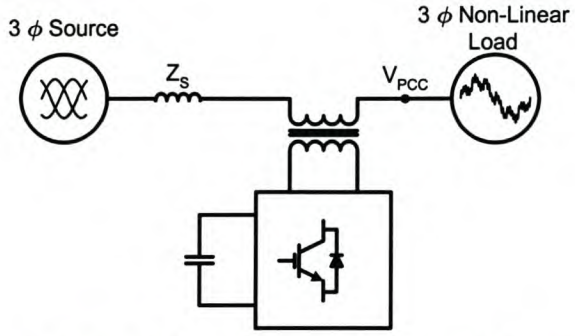


Figure 3-25: Active Series Compensation

The basic operation of the series compensator is best explained by considering Figure 3-26. The main objective is to try maintaining a receiving-end voltage, V_R, at the same magnitude as that of the sending-end voltage, V_S.

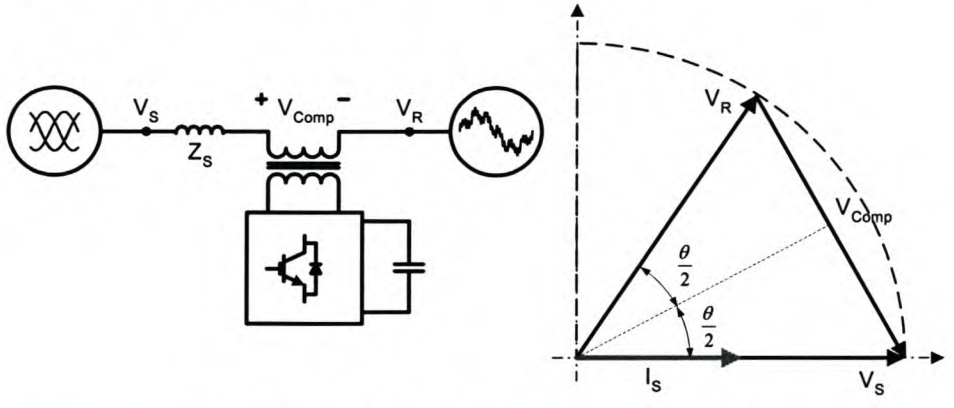


Figure 3-26: Active Series Compensation Explanation

This is achieved by injecting a series voltage, V_{Comp}, onto the power network. The magnitude of the compensating voltage is calculated using the circle diagram, a segment of which is shown in Figure 3-26. As can be seen, both V_R and V_S are kept at the same magnitude when

using this method [23][24]. Firstly, one of two possible compensation priorities has to be decided upon. The rating of the compensator is limited by either the magnitude of the compensating voltage, or alternatively, the maximum phase shift required to be compensated for. While the compensation voltage is the deciding factor, it is possible to calculate the maximum obtainable phase shift that the series device can compensate for by using (3.4).

$$V_{Comp} = 2 \times V_S \times \sin\frac{\theta}{2} \tag{3.4}$$

The series compensator absorbs non-active current and a lesser magnitude of active current from the load current flowing to the load. The non-active currents oscillate between the line and the DC bus capacitors, in the same fashion as previously explained. It is this action that enables the series compensation. The active power flowing through the series filter is ultimately returned to the system.

The series compensator is represented as a voltage source in its equivalent circuit, Figure 3-27. For the series filter, the Thevenin equivalent circuit represents the load, and in this case it is a voltage-source harmonic load.

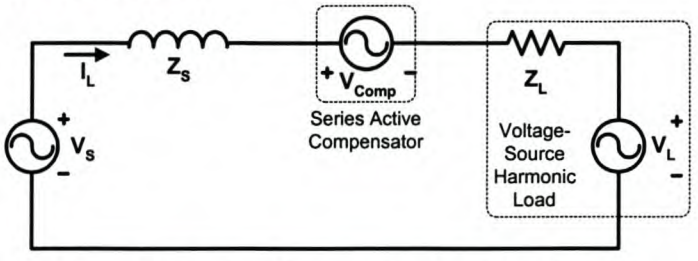


Figure 3-27: Series Compensator Equivalent Circuit

For the series filter [21], the circuit equations have shown that they are better suited for voltage-source harmonic loads. When trying to compensate for the harmonic currents of a current-source harmonic load, the series device requires small harmonic impedances on the source, Z_S, and load side, Z_L. However, current-source harmonic loads are characterised by their large harmonic impedance. This results in an infinitely large compensating voltage required from the series filter. It is for this reason that the series device is not suited for typical thyristor rectifier loads. The circuit equations in [21] further show that that when dealing with voltage-source harmonic loads, the characteristics of the series filter are independent of the source impedance, Z_S, and the load impedance Z_L, making it very effective in suppressing harmonics in the source current.

In conclusion, the series active filter provides dynamic compensating capabilities, far exceeding the capability and benefits of static series compensators. Furthermore, they are suited to mitigation of harmonics of voltage-source harmonics, as opposed to the shunt compensator, which is in turn suited to current-source harmonics.

Although this functionality is not related to any traction or MVDC application, the converter topologies compared in this thesis are fully capable of performing this task.

3.3.1.3 Active Series-Shunt Compensation

Finally, the last of the active filter combinations is that of the series-shunt topology, seen in Figure 3-28.

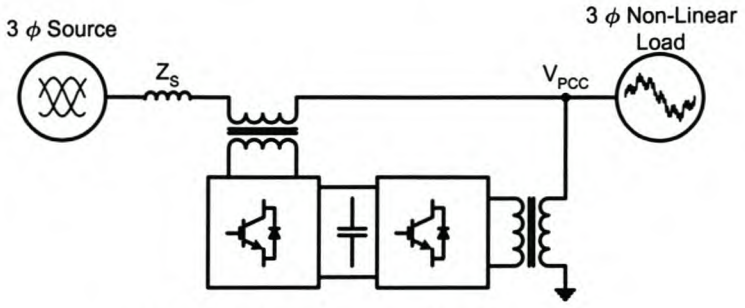


Figure 3-28: The Series-Shunt Topology

This topology encompasses the best capabilities of both the previously discussed topologies [16][25]. Furthermore, it is capable of performing dip compensation during fault conditions, a capability that the series in-line device is only capable of performing when supplied with some form of energy storage on its DC bus. Absorbing active power via the shunt connection, energy is supplied to the DC bus. The series compensator, to maintain the system voltage, subsequently uses the DC bus energy.

It must be noted that the extent of the dip compensation is again dependent on the system rating. The main disadvantage is again the increased component count; however, the ratings can be reduced, unlike that of the in-line device.

3.4 Chapter Summary

This chapter has investigated the various basic compensation schemes for enhancing performance and network conditions of typical traction and MVDC applications. This includes the various power quality concerns that need to be mitigated in order to ensure minimum system pollution, whilst performing the specified tasks. The benefits of using MVDC are seen in the extending of the power network, while still being able to perform power factor correction. The converter solutions not only perform the required functions well but also do so more efficiently and with less power system pollution. The versatility of the applications is enhanced. A wide range of general power system support, not previously available, is thus possible. This chapter clearly shows the superiority of the active devices over their passive counterparts. With this foundation present, the next chapter can be dealt with, where multilevel topologies are investigated. The performance of multilevel converter topologies, and more specifically the SSC and NPCC topologies core to this thesis, can now be evaluated as potential candidates for traction and MVDC applications.

Chapter 4 Multilevel Converters

4.1 Converter Limitations and Proposed Solutions

This chapter discusses the limitations of the switching devices within the standard Graetz-Bridge converter topology. As mentioned in the introductory chapter, various switches are available for use, but each of the silicon switches has its limitations. The first of the limitations is the switching frequency at which they are capable of operating without the turn-on and turn-off times being compromised. The next limitation is that of the switch power ratings. Each type of silicon switch has a blocking voltage limit, after which the silicon insulation fails. This is due to the architecture of the device and the material used. Silicon is not tolerant of over-voltages, even for short periods of time. The current limitation is dependent on the switched current magnitude, as well as the switching frequency at which it operates. Low switching frequencies combined with effective heat extraction allow the switch to operate at a higher than rated current rating, for very short periods of time.

There are two approaches available when operating at high power. The first is the paralleling of a number of IGBT switches, increasing the rated switch current. Manufacturers do this within IGBT modules to increase their current ratings. During turn-off, parallel IGBTs need to turn off at the same time, otherwise the slower IGBTs break the full load current, resulting in the destruction of the switch. The drawback of high power operation, using low voltages and high current, is that the current ratings of all the other converter components become excessive. Excessive currents at high-frequency cause high losses and component overshoot. Large step-down transformers are thus required when operating on high voltage power networks.

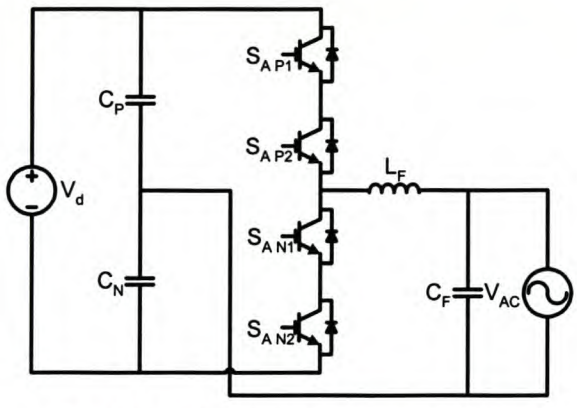


Figure 4-1: Switches Connected in Series

The preferred solution to high power switching is to increase both the operating voltage and current levels. Depending on the application and the technology requirements, current and voltage levels are normally trade-offs between losses, insulation levels and filter component sizing. This implies operating at high DC bus voltage and load/source voltage levels. To do this, switches are connected in series to effectively create one high voltage switch, Figure

4-1. Individual switch voltage limitations are thus not exceeded and converter components requiring higher voltage ratings are simply connected in series as well. The series IGBT connection still requires all of them to switch off at the same time, otherwise the voltage limit of some of the IGBTs will be exceeded, resulting in their destruction. This factor is subsequently the largest concern as switch turn-off times are not always identical.

4.1.1 Voltage Balancing of Series Connected Switches

One solution is to use perfectly matched devices, the closest matches being IGBTs manufactured from the same batch [73]. The disadvantage is that in the event of a switch failure it would require the replacement of the entire series string, a very expensive option. Another solution is using Collector Emitter Voltage Feedback. This solution forces the collector emitter voltage to follow a predetermined reference voltage, controlling the turn-on and turn-off times of the switches. Various control methods exist [27], but all control voltages are chosen to suit the slowest switch, ensuring voltage sharing between the strings of series switches. An advantage of this technique is that it enables snubber-less operation. A disadvantage is the increased switching losses when compensating for the slowest switch.

Bootstrapping [73][67] of the gates also ensures synchronous opening of the switches. This method level shifts the gate signals using diodes and dividing circuits. The advantage is its low cost, while the disadvantage is the high losses that increase with the number of switches connected in series. Overall the efficiency is low.

A further alternative to voltage sharing is using RCD snubber circuits connected across a switch [73]. The snubber, consisting of a resistor, capacitor and diode, allows the turn-off energy to be stored in the capacitor. The capacitor discharges through the resistor while the switches are on. The snubbers ensure slow voltage rise times during turn-off, by absorbing the energy that would ordinarily have been dissipated in the switch. The design parameters ensure the switching slope is reduced to that of the slowest switch, ensuring voltage balancing over the series string.

4.1.2 High Voltage Switching Observations

The merits of switching at high voltages are high power operation. However, the quality of the switched waveform and the impact on the system components are just as important as the magnitude. Switching voltages in the kilovolt range results in high *dv/dt*'s being generated across the filter inductor. These high *dv/dt*'s require the inductor size, used to shape the waveform, to be large, thus increasing their costs. If small impedance inductors are used, noisy current waveforms are generated. Control using a current regulator is also complicated when the current ripple is extremely large.

These high voltage devices create a further problem when examining loading conditions of the converter [28]. In many cases loads and motors are supplied via a cable. The shunt capacitance (from the insulation forming a dielectric) and conductor inductance of the cable re-

sult in a series string of LC filters. The high voltage *dv/dt*'s are amplified on the cable; the longer the cable, the larger the *dv/dt*. By examining converters with two series switches and a DC link voltage of 3.3 kV, data has shown that a *dv/dt* of up to 12 kV/μs is propagated on the cable at the respective switching frequency. This stresses the equipment insulation on the end of the cable. The IEC 34-17 standard for medium voltage machines considers 500 V/μs [28] as acceptable. The problem is also evident when the converter acts as a frequency drive to large motors [29], where the load frequency is adjusted. These factors have led to alternative topologies being developed and the solutions are in the form of multilevel converters.

4.2 Multilevel Converters

Multilevel converters consist of a multiple of the usual six switches found in a normal three-phase inverter. Higher power and voltage ratings are achieved by the sharing of the Volt-Amperes by the switches, be it in series or in parallel. The topologies have high DC link voltages, without the problems associated with the series connection of switches. They also create stepped voltage output levels during switching. Lower *dv/dt*'s are experienced over the inductors, thereby reducing the harmonic content. A further benefit is the cost and size reduction of the inductor for a given dynamic response.

The large number of switches available allow for an increased freedom in the switching algorithms and switching states. This factor permits the variation of the dynamic compensation capabilities. A further advantage is the increase in the apparent switching frequency, made possible by the staggering of gating signals between the multiple levels within the converter [28][32][33]. Switching harmonics thus appear at higher frequencies, since they occur as sidebands of the apparent switching frequency. With this in mind the various multilevel converter topologies are examined.

4.2.1 The Flying Capacitor Multilevel Converter

4.2.1.1 Topology

The flying capacitor multilevel converter, first introduced by Meynard [7], is the first of the multilevel converters to be discussed. This topology enables operation at high DC bus voltage levels, increasing the converter's overall power rating. It uses series connected switches, like those seen in Figure 4-1, but makes use of the "flying capacitor", C_1 seen in Figure 4-2, to share the voltages over the switches and prevent the voltage ratings from being exceeded. Figure 4-2 is a single-phase three-level converter and is used for operational explanation. Typically more switches and clamping capacitors are used, allowing for operation at higher DC bus voltages and increased stepped output voltage levels; however, explanation of its operation becomes complex.

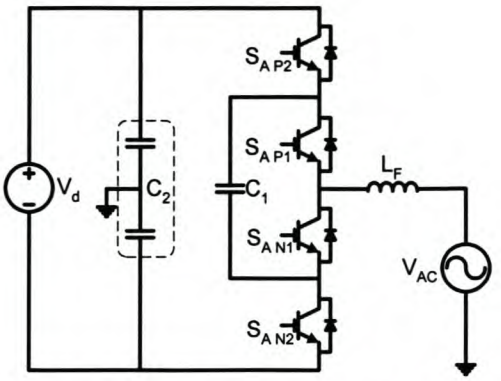


Figure 4-2: The 3-Level Flying Capacitor Multilevel Converter

The floating capacitor, C_1, "clamps" the voltage over the series switches, by way of the capacitor divider circuit. This implies that the voltage over opened switches is kept constant. The voltage to which open switches are exposed can be calculated using (4.1).

$$V_{switch} = \frac{V_{dc}}{N} \tag{4.1}$$

Where N is the number of cells, and in the case of Figure 4-2, this would be 2. A cell consists of one capacitor and two switches, seen as the shaded area of Figure 4-3(B). Figure 4-3 is an alternative representation of Figure 4-2. Thus we can determine the number of cells required for a given DC bus voltage, while using switches with specific voltage limits.

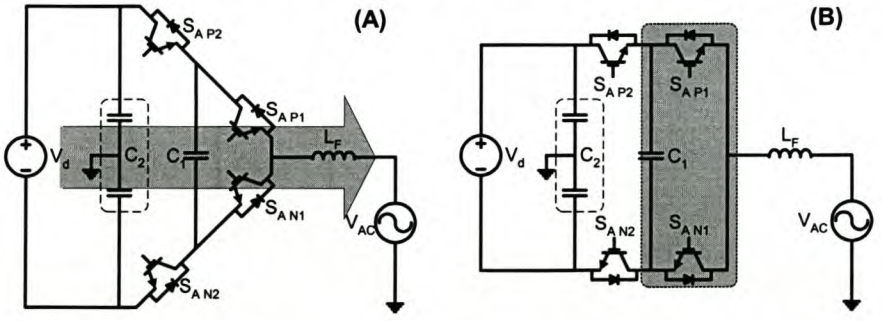


Figure 4-3: Alternative Shape of a 3-Level Flying Capacitor Multilevel Converter

Unlike the switches, the capacitors are exposed to increasing voltages as the number of cells increase [7]. These voltages can be calculated using (4.2).

$$V_{Cap\,x} = \frac{V_{dc}}{N} \times k \tag{4.2}$$

Where: k = cell number

N = number of cells

4.2.1.2 Waveform Generation

For the flying capacitor topology, Figure 4-2, complementary pair switching is used. Switches $S_{A\,P1}$ and $S_{A\,N1}$ form one complementary pair, while switches $S_{A\,P2}$ and $S_{A\,N2}$ form the other. This implies that when one switch is on, its complementary switch is off. The complementary pairs are situated around the flying capacitors, the reason being that if both switches were on at the same time, the capacitors would be shorted out.

By analysing the switching states, the output voltage waveforms of this converter can be realised. Figure 4-4 shows all the possible switching states available when using the complementary switching. In Figure 4-4 the shaded switches are defined as off. It can be seen that for the three-level converter, three possible output levels exist, 0V, $\frac{1}{2}V_d$ and $-\frac{1}{2}V_d$. $-\frac{1}{2}V_d$ is applied to the AC side while operating in State 1, connecting the output to the negative DC rail. In State 1, C_1 is effectively removed from the circuit. Similarly $\frac{1}{2}V_d$ is applied to the AC side when switching the converter into State 3, connecting the output to the positive DC bus rail.

It is the other two states that are of interest as they best explain the operation of the flying capacitor C_1, emphasising the uniqueness of this topology. During State 2, the flying capacitor is connected between the output and the negative rail. The two capacitor voltages oppose each other, resulting in an output voltage of 0V. But in switching State 4, the capacitor is connected to the positive DC bus. The sum of the two voltages again results in 0V being applied to the load. The primary difference between the two states is that the current flow through the capacitor C_1 changes direction.

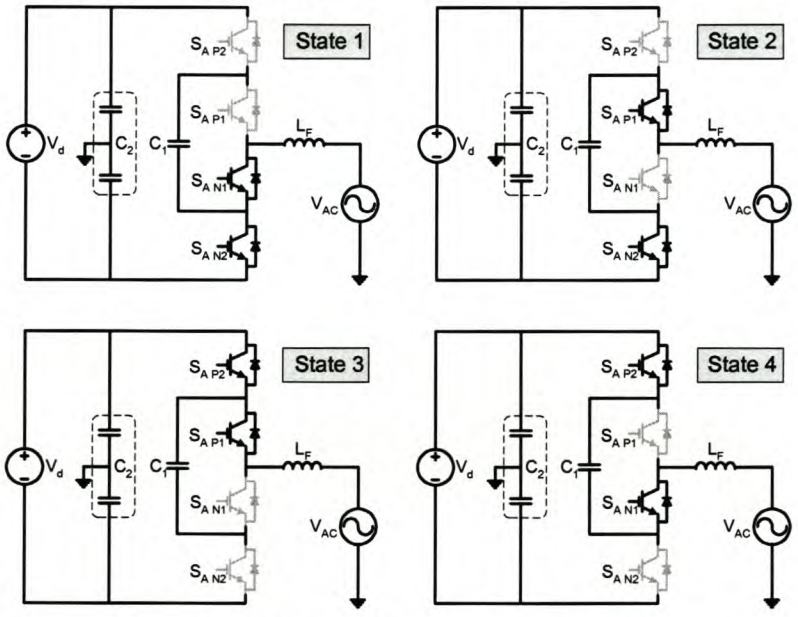


Figure 4-4: The Flying Capacitor Switching States

Simulated waveforms of this mode of switching are seen in Figure 4-5.

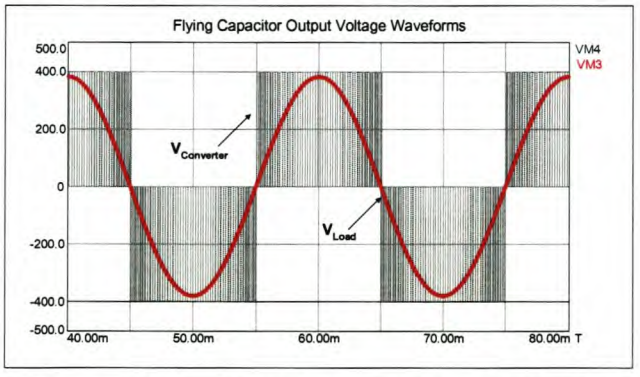


Figure 4-5: Stepped Output Voltage Waveforms of a 3-level Flying Capacitor Converter

A stepped output voltage waveform is observed. This is one of the largest benefits of multilevel switching, resulting in lower *dv/dt*'s, mitigating the problems associated with series connection of switches. In the flying capacitor topology the stepped output voltage levels are a product of the number of flying capacitors. Re-examining states 3 and 4, it can be seen that if only one of these states is used, the flying capacitor cannot maintain its voltage, since it would discharge at the following rate:

$$ic = Iout = C\frac{dVc}{dt} \tag{4.3}$$

To recharge the capacitor after discharging, it is necessary to use both states, ensuring the output stays constant. Recharging need also not occur immediately, and can be performed over a number of switching periods, by simply extending the switch state times.

4.2.1.3 Topology considerations

4.2.1.3.1 Effects of Harmonics

Harmonics generated during switching form as sidebands of the switching frequency [68]. Besides affecting the output power quality, these harmonics also affect the DC link capacitors. For the capacitors, the average current through them must remain zero for them to maintain their charge value. Dominant harmonics, generated during switching, recur over a period of time and if there is no harmonic cancellation, it results in the collapsing or boosting of the capacitor. This condition degrades the flying capacitor's performance and results in the control of the converter becoming more complex. Phase shifting of the control signals of the different levels stabilises this condition. The size of the phase shift influences the harmonic spectrum of the output voltage. When using a three-cell converter, a phase shift of 120° between the different control signals would effectively eliminate the more dominant harmonics prevalent in each cell [30][31]. The required phase shift is calculated using (4.4).

$$Phase\ \ Shift = \frac{2\pi}{N} \tag{4.4}$$

Large phase shifts in the control signals require large DC capacitors. To reduce the capacitor values required, a smaller phase shift could be considered. However, this would require more cells in the converter, increasing the component count. Alternatively, the increase in cells leads to a higher voltage range and/or a supply with smaller magnetic components and less harmonics.

4.2.1.3.2 Capacitor Design

Obtaining the optimum capacitor size for this topology is a complex task. The ripple voltage and the RMS current through the capacitor have an impact on the sizing of the capacitors. Each capacitor, being switched into the circuit, reacts differently and is not affected by other cells. Using the capacitors' switching states and the resultant output waveform, it is possible to derive various equations for the ripple voltage and the RMS current during the switching

period. It is then possible to determine the required capacitor value for a given maximum ripple voltage [32]. The formula in question is as follows:

$$Ck > \frac{\varphi \times Id}{2\pi fs \times \Delta Vck\,\max} \tag{4.5}$$

Where: k is the cell number

φ is the phase shift in radians

f_s is the switching frequency

$\Delta V_{ck\,max}$ is the maximum ripple voltage

I_d is the load current

The equations derived for the ripple voltage and RMS current are used to plot graphs to determine the optimum values for a given system. Models have been developed to linearise these converters since they cannot be modelled using normal state space averaging. The system is non-linear due to its configuration. Transient behaviour of the converter is affected by the phase shifting of control signals and the current harmonics that the converter experiences [31].

4.2.1.3.3 Three-Phase Converter Considerations

An important consideration for the three-phase converter unit, Figure 4-6, is that of component count. Examining the DC bus of the three-phase flying capacitor converter, it is evident that the extra flying capacitors on each phase increase the overall component count of the topology.

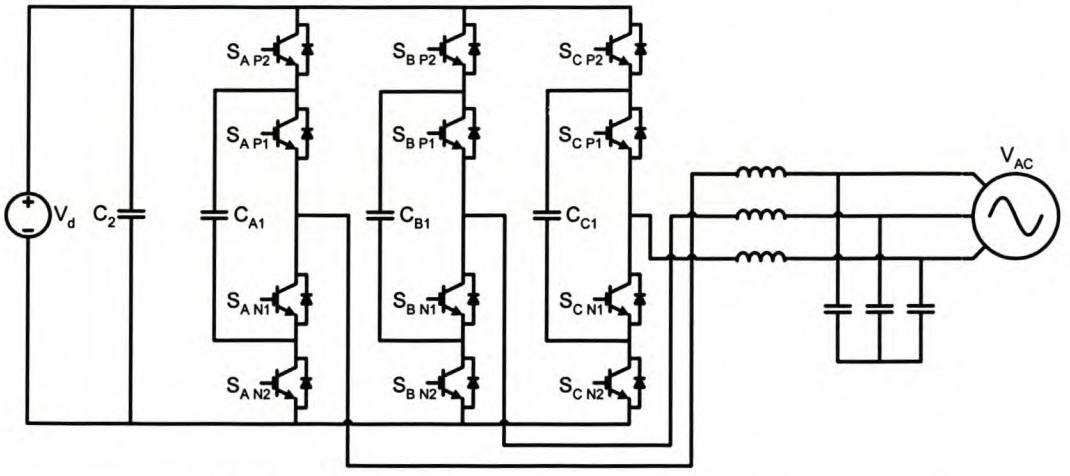


Figure 4-6: Three-Phase 3-Level Flying Capacitor Converter Topology

Furthermore, calculating the ratings of these capacitors, as previously discussed, is not trivial. The flying capacitors also need to be mounted physically close to the switches in order to reduce the parasitic inductance paths during switching. The DC bus design, along with the complex switching techniques used to ensure that the capacitors remain charged, are important factors requiring consideration when choosing this topology.

4.2.1.4 Topology Advantages

The advantages are as follows:

- This converter is capable of switching at a high apparent switching frequency, reducing the switching harmonics.
- In this topology, the harmonics can be further reduced by phase shifting the control signals, a technique also known as interleafing.
- The number of stepped output voltage levels is easily increased by the addition of extra cells. This further facilitates the reduction of the magnetic ratings.
- The large number of capacitors used in the cells gives this topology a good dip ride-through capability.
- This topology enables dynamic capacitor and output voltage level balancing.
- Modulation and/or regulation of real and reactive power are possible.

4.2.1.5 Topology Disadvantages

The disadvantages are:

- The high number of capacitors required, with increasing voltage ratings, increasing the cost and size of the topology. Overall a high capacitor component count.
- The controlling and modelling of the converter is relatively complex.
- Modelling and design of the converter is complex.
- Flying capacitors need to be mounted very close to the switches of the respective cell in order to reduce parasitic inductance paths during switching.
- Three times the number of flying capacitors are required during three-phase operation. The extra phases cause the aforementioned disadvantages to be compounded.

4.2.2 The Cascaded H-Bridge Multilevel Converter

4.2.2.1 Topology

This cascaded H-bridge multilevel topology, introduced by Hammond [9] and seen in Figure 4-7, enjoys much popularity, primarily due to its modularity and versatility. It is capable of switching output waveforms with a number of stepped output voltage waveforms, reducing the harmonic content. Like other multilevel topologies, individual switch voltages are restricted, enabling the series connection of switches required for high voltage operation. Its modularity results in a low component count, compared to other topologies; another feature that makes it attractive.

Examining the five-level converter structure, Figure 4-7, the following aspects of the topology are observed. The single-phase structure is constructed by the series connection of standard full-bridge converters. This is obtained by connecting the output, the centre point of one of the phase-arms of the lower converter, to the centre point of one of the phase-arms of

the upper converter. The lower converter is grounded via the centre point of the "free" phase-arm, while the converter output is from the "free" phase-arm of the top converter. Each of the modules is capable of obtaining three output voltage levels, $+V_d$, $-V_d$ and 0V. Obtaining the $+V_d$ and $-V_d$ is made possible by the ground connection to one of the phase-arms, enabling the DC bus to be swung around it.

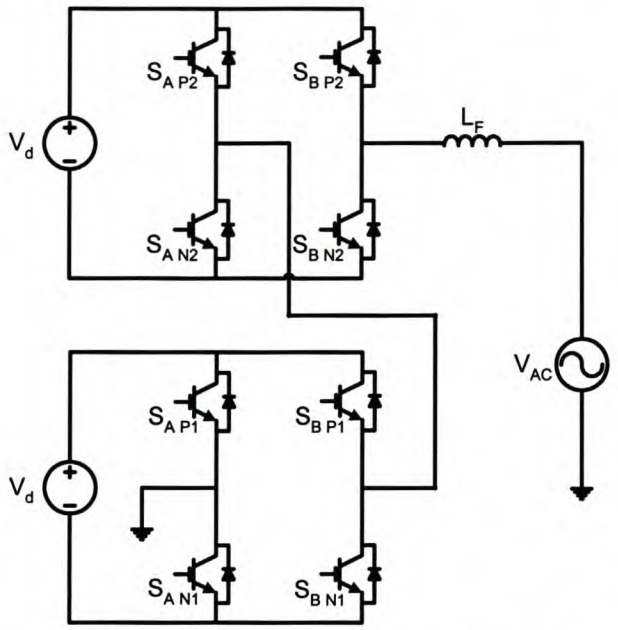


Figure 4-7: The 5-Level Cascaded H-Bridge Converter Topology

More levels are easily added to this topology in this manner. Subsequently, a converter with m levels would consist of N_H full-bridge converters, according to (4.6).

$$N_H = \frac{(m-1)}{2} \tag{4.6}$$

The largest divergence from other multilevel topologies is that the cascaded converter requires separate DC sources for each single-phase full-bridge converter when modulating waveforms [34][35]. Alternatively they can be replaced with capacitors for static VAr generation applications [36][37].

4.2.2.2 Waveform Generation

As is the case with most converters, the switches are operated as complementary pairs when generating waveforms. In Figure 4-7 switches $S_{X\,Py}$ and $S_{X\,Ny}$ are complementary, with X denoting the phase-arm and y the converter level, preventing the shorting out of the DC bus. The numerous switching permutations of the converter are somewhat different from the other multilevel converters. This is also known as Step Modulation [34]. Figure 4-8 shows the possible switching states of the five-level converter, and their associated stepped output voltage.

Dark switches symbolise closed switches while shaded switches symbolise open switches. Working through states 1 to 5, an understanding is gained of how the isolated DC sources are connected to the AC supply on the output. The shaded output voltages for each state are also shown.

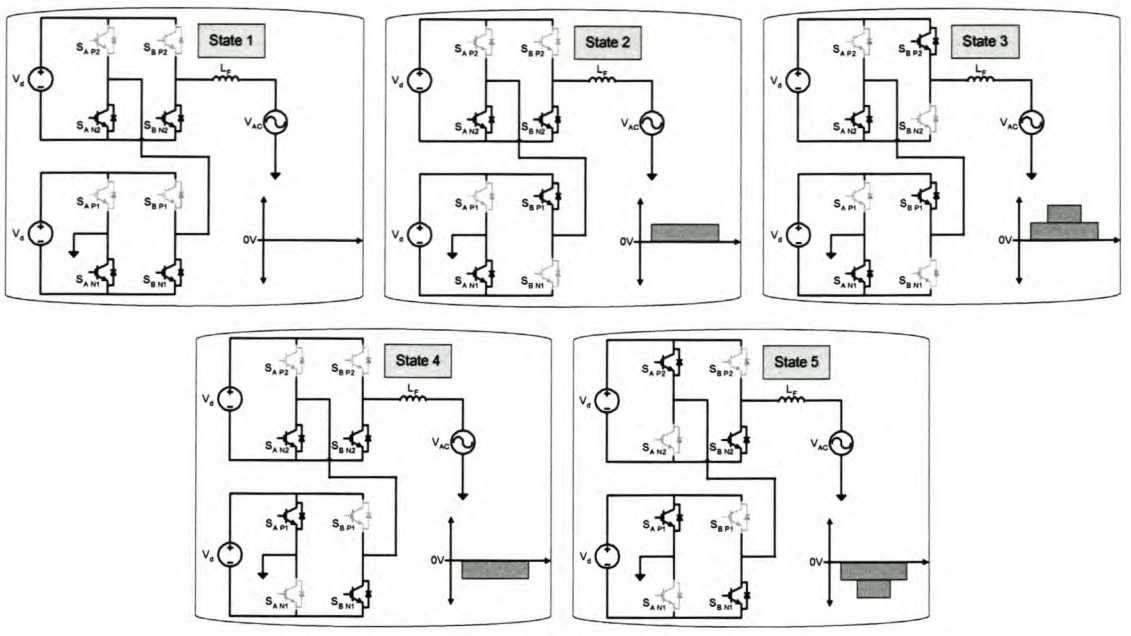


Figure 4-8: The Cascaded H-Bridge Switch States

The waveforms of states 3 and 5 are double the size of states 2 and 4 respectively, since the two DC sources sum to apply $2V_d$ and $-2V_d$ to the load. It is clear from Figure 4-8 that double the total DC source voltage can be applied to the load by "swinging" the DC sources around the ground terminal. This feature is a great asset to the topology.

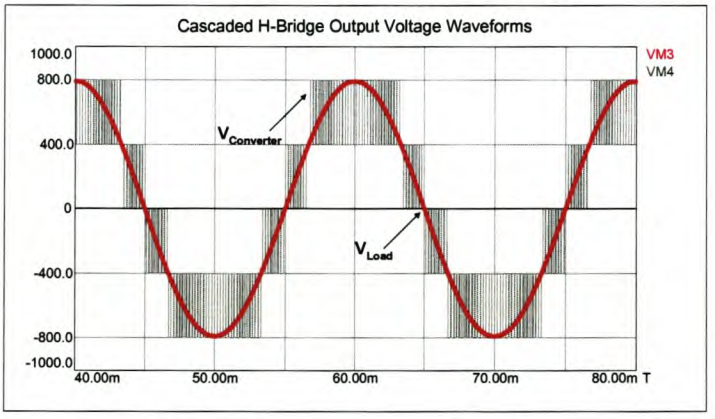


Figure 4-9: Stepped Output Voltage Waveforms of a 5-Level Cascaded H-Bridge Converter

The switching states of Figure 4-8 yield output voltage waveforms like those simulated in Figure 4-9. The simulation model uses 400 V isolated DC sources, resulting in a staircase waveform ranging between 800 V and -800 V. To achieve the same number of stepped output voltage levels as that of the flying capacitor topology, only one H-Bridge converter is required. In the generation of the staircase waveform, specifically for the three-phase inverter, the following formula holds true:

$$V_{AC}max = \sqrt{\frac{3}{2}} \times \frac{4}{\pi} \times N \times Vd \tag{4.7}$$

Where N is the number of series H-bridge cells and the switching phase angles are equal to zero [36].

4.2.2.3 Topology Considerations

4.2.2.3.1 Device Limitations

Although device operation is simple, the largest drawback is that it requires an isolated DC power source. This is typically a rectified supply being fed from an isolation transformer, with as many isolated outputs as there are levels in the converter. These types of transformers are non-standard and increase the cost of the converter considerably. Other size reducing alternatives to the isolated transformer supply also exist, one being the usage of bi-directional DC-to-DC converters, fed off a common DC bus.

The cheapest alternatives are passively rectified DC sources, but this prevents the converter from four-quadrant operation; regeneration is not possible. Using a DC dump is one solution to dissipate the energy build-up by regeneration; however, it requires control and the energy loss is not preferred. Active rectifiers are also an alternative, but they also require an isolated power source fed from a transformer, once again increasing the cost [35].

Batteries provide another alternative, having the converter store the energy until required. This would only be feasible when the converter is typically being used as a dip compensator, where continuous operation is not required.

Using just capacitors makes the converter a very attractive option for applications such as an SVC or an active power filter where only reactive power is required [36][37]. The drawback here is that the full rating of the converter is not always required, resulting in the discharging of some of the capacitors and not the others, and uneven power sharing. During this period of low usage the losses of the converter are high. Here it is up to the control algorithm to ensure the balancing of the voltages on the capacitors. One suggestion for the mitigation of this condition is that of random cell usage. Numerous suggestions for optimised control have also been suggested [38].

4.2.2.3.2 Switching Alternatives

PWM techniques as well as vector modulation are viable switching alternatives. Phase shifting in the carrier or reference signals often results in reduced harmonics and better switch utilisation. It could also be employed for better charge control of capacitors or batteries, if they are indeed used. The phase shift, as always, is dependant on the number of output voltage levels [34]. Unfortunately PWM techniques introduce more switching losses due to the high switching frequency. With this in mind alternative methods have been sought. By reviewing the switching states and the subsequent waveform generation of a three-cell converter, seen in Figure 4-10A, one sees that the switch utilisation of the top cell is relatively low. Gating each cell in the converter for the same period of time, but staggering them, obtains improvement of the switch utilisation. The switch timing changes, and the basic idea is seen in Figure 4-10B. This technique causes significant stress on the anti-parallel diode of the first cell.

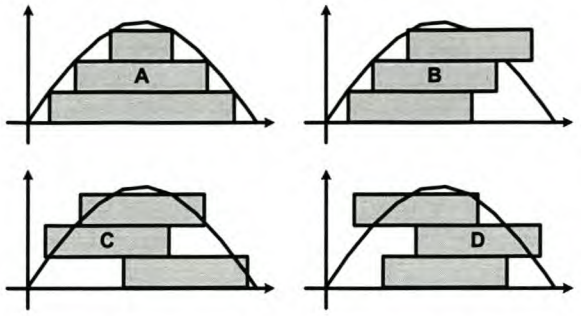


Figure 4-10: Alternative Switching for Waveform Generation

A solution is to cycle the gating pulses like those seen in Figure 4-10C&D.

4.2.2.3.3 Three-Phase Converter Considerations

Construction of a three-phase three-level device, Figure 4-11, requires the addition of two more phase-arms.

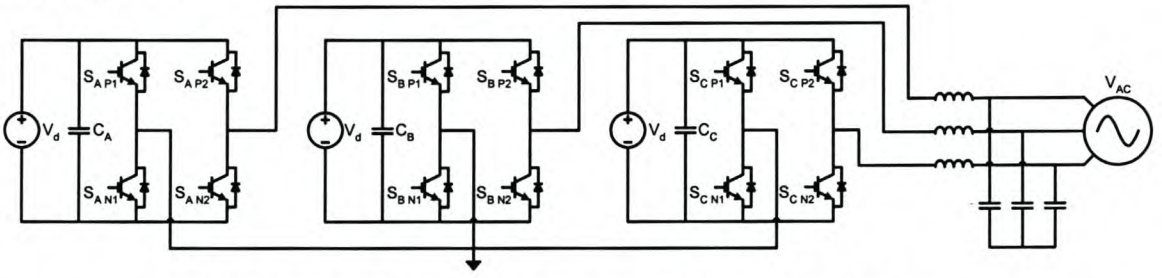


Figure 4-11: Three-Phase 3-Level Cascaded H-Bridge Converter Topology

This is where the cascaded H-bridge topology is at a disadvantage. Each full-bridge phase-arm has to be replicated three times. Furthermore, each of the individual phase-arms requires its own isolated power supply. Although the same number of switches is used as for the three-level flying capacitor, the three extra isolated power supplies and their associated components increase the overall component count and cost of the topology. A further increase in component requirements is expected if bi-directional operation is required.

4.2.2.4 Advantages

The advantages are as follows:

- This converter is capable of switching at a high apparent switching frequency, reducing the switching harmonics.
- Phase shifting the control signals further reduces harmonics.
- With a significant number of stepped output voltage levels already at its disposal, the increasing of levels is easily achieved by the addition of extra H-Bridges, further reducing the magnetic ratings.
- For single-phase devices, it has the lowest component count of the multilevel topologies.
- It is modular in its structure.
- The control is not complex, and soft switching is easily possible.

4.2.2.5 Disadvantages

The disadvantages are:

- When contributing real power, isolated DC power sources are required, increasing the topology's overall cost.
- The component count increases dramatically for three-phase applications, making it comparable, and in some cases worse, than other topologies.
- Bi-directional power flow increases the price as well as the control requirements of the topology.
- Random system disturbances make it difficult to decide on a switching sequence.

4.2.3 The Diode Clamped Multilevel Converter

4.2.3.1 Topology

Another of the multilevel topologies is the diode clamped converter, first introduced by Akagi and Nabae [8]. Figure 4-12 shows the topology, which enjoys widespread usage in industry, especially in the field of motor control.

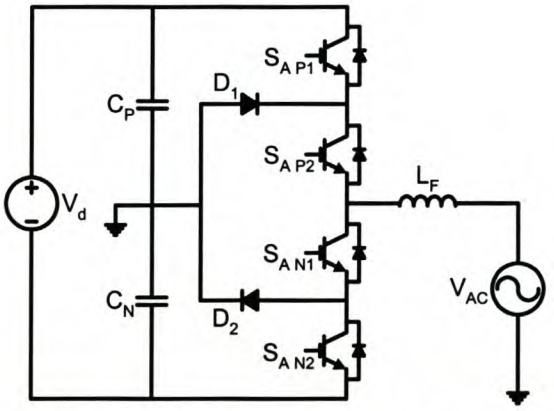


Figure 4-12: The 3-Level Diode Clamped Converter Topology

The three-level diode clamped converter in Figure 4-12 is also known as the Neutral Point Clamped Converter (NPCC). The converter has an even number of switches and diodes. The number involved, however, is determined by the number of output voltage levels, *N*, chosen for the converter and required by the load [8][37][39]. These stepped voltage levels are obtained by the interaction between the clamping diode pairs, D_1 and D_2, and the capacitor dividing circuit, created by C_P and C_N in Figure 4-12. The diodes also create freewheeling paths for the inductor currents. The addition of extra voltage levels is realised by the addition of clamping diodes, capacitors and switches. A typical four-level converter structure is seen in Figure 4-13. Each converter comprises (*N*-1) capacitors and the number of switches in each phase-arm is calculated using (4.8). The number of diodes required is calculated using (4.9) [40].

$$No\ of\ switches = 2\times(N-1) \tag{4.8}$$

$$No\ of\ diodes = 2\times(N-2) \tag{4.9}$$

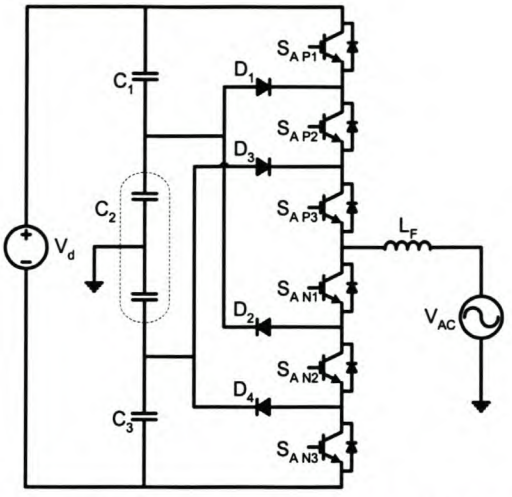


Figure 4-13: A 4-Level Diode Clamped Converter

4.2.3.2 Waveform Generation

The diode clamped converter uses a different type of complementary switching technique to those of the previously discussed topologies. In Figure 4-12, switches $S_{A\,P1}$ and $S_{A\,N1}$ form one complementary pair while $S_{A\,P2}$ and $S_{A\,N2}$ form the other. Using these switching states, the various combinations are shown in Figure 4-14.

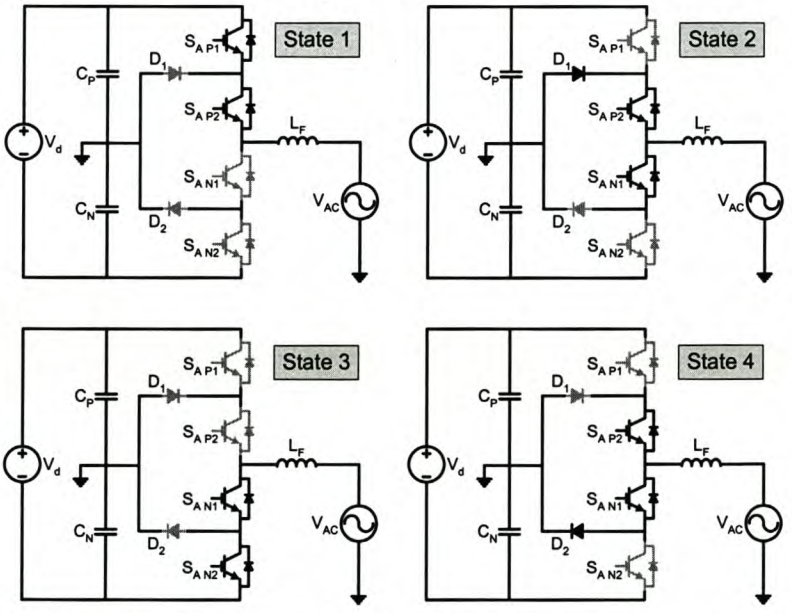


Figure 4-14: The 3-Level Diode Clamped Converter Switching States

Once again the shaded switches imply that the switch is turned off. During State 1, $\frac{1}{2}V_d$ is applied to the AC supply. During State 2, switch $S_{A\,P1}$ is switched off, and diode D_1 becomes forward biased, creating a freewheeling path for the inductor current. This state is defined as a "zero state", since no driving voltage, positive or negative, is applied to the load, much like unipolar switching. The diode D_1 also ensures that capacitor C_P's voltage is the only voltage that is applied to the open switch $S_{A\,P1}$.

During State 3, switches $S_{A\,N1}$ and $S_{A\,N2}$ are closed and $-\frac{1}{2}V_d$ is applied to the output. This state is used when modulating the negative half of the required waveform. Finally State 4

creates the freewheeling path for State 3. Once again the opened switch $S_{A\,N2}$ is only exposed to $-\frac{1}{2}V_d$, capacitor C_P's voltage.

Using this technique, a staircase output waveform is modulated like that of the simulated waveforms shown in Figure 4-15. The output waveform resembles that of the flying capacitor topology, with the output voltage ranging between 400 V and –400 V, while operating at a DC bus voltage of 800V.

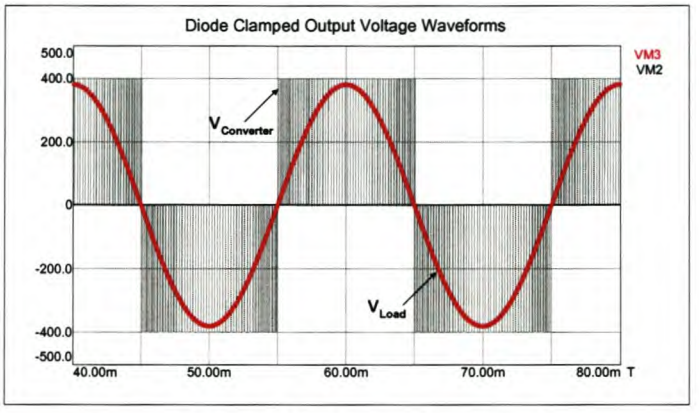


Figure 4-15: Stepped Output Voltage Waveforms of a 3-Level Diode Clamped Converter

4.2.3.3 Topology Considerations

4.2.3.3.1 Four-Level and Higher Capacitor Discharge Criterion

When using a multilevel converter, like that seen in Figure 4-13, with more than three output voltage levels, DC bus capacitors are isolated from the positive and negative DC rails, in this case C_2. For the capacitors to keep their output voltage constant it is necessary for the average current through the capacitors to be zero. During inverting mode, real power is supplied to the load. This results in capacitor C_2's voltage decaying to zero volts. The opposite is true during rectification, except that the voltage rises until it is clamped at the DC bus voltage, compromising switch ratings and the stepped waveform. If the converter is used to supply loads where the current is 90° out of phase with the voltage waveform [37], this problem is remedied, making it an ideal solution for SVC applications.

Boost rectifiers could be employed to regulate the capacitor voltages; however, this increases the cost, complexity and component count. Alternatively, back-to-back operation would result in the converter being immune to this problem, with one converter rectifying and the other inverting.

4.2.3.3.2 Diode Ratings

Re-examining Figure 4-13 shows that when switches $S_{A\,N1}$ to $S_{A\,N3}$ are closed, diode D_2 is forced to block the summed voltage of capacitors C_2 and C_3. This shows that the voltage ratings of the diodes increase, as the number of levels increase. A *N*-level converter will have two diodes that are exposed to a blocking voltage calculated using (4.10).

$$V_{diode} = \frac{N-1-k}{N-1} \times Vd \tag{4.10}$$

Where N is the number of levels and k is a numerical value that goes from 1 to N-2 with V_d being the total DC link voltage [7]. Usually diodes of similar rating to the switches are used, requiring a number of them to be connected in series to perform the blocking. If the number of levels gets too high, construction will become impractical. Furthermore snubbers over the diodes might also be required to compensate for stray parameters.

4.2.3.3.3 Three-Phase Converter Considerations

The addition of two phase-arms results in the three-phase converter topology, like that represented in Figure 4-16. The first observation about this topology is the high number of diodes required, increasing the topology's component count.

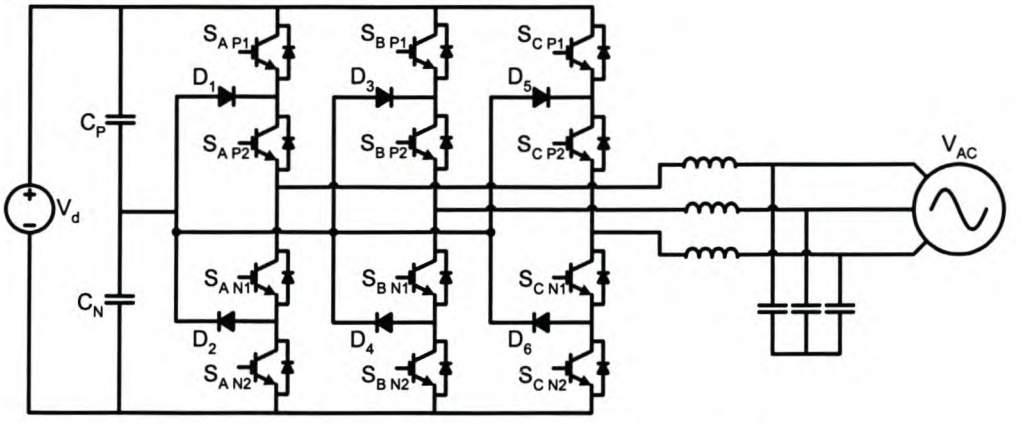


Figure 4-16: A Three-Phase 3-Level Diode Clamped Converter

Secondly, the converter is connected to a three-phase supply on its output. The load is thus a coupled connection and any switching in one phase-arm affects the waveforms of the other two phases. It is not feasible to control this converter using the technique used on a single-phase converter. Three-phase control is complex and requires the use of a modified space vector control technique [41].

4.2.3.4 Advantages

The advantages are as follows:

- Numerous stepped output voltages can easily be realised, reducing the current ripple and switching harmonics, further resulting in reduced magnetic ratings.
- Simple construction and design.
- Back-to-back operation is possible, sharing the DC bus capacitors.
- Losses within the converter are low since the converter is capable of switching at the fundamental frequency of the output waveform.
- Operation as a reactive power compensator does not affect its capacitor voltages.

4.2.3.5 Disadvantages

The disadvantages are:

- The number of diodes becomes large when the number of the output voltage levels is increased, increasing the component count significantly.
- When using more than three output levels, power flow control is problematic. The capacitor draining and charging requires alternative solutions and extra control.
- The extra diodes introduce extra parasitic components, requiring them to be placed as close as possible to their appropriate switch.
- Three-phase operation increases the diode count and the control technique is more complex.

4.2.4 The Series-Stacked Multilevel Converter

4.2.4.1 Topology

The last of the multilevel converter options to be discussed is the 2-level series-stacked converter (SSC) [10][35] [42], seen in Figure 4-17.

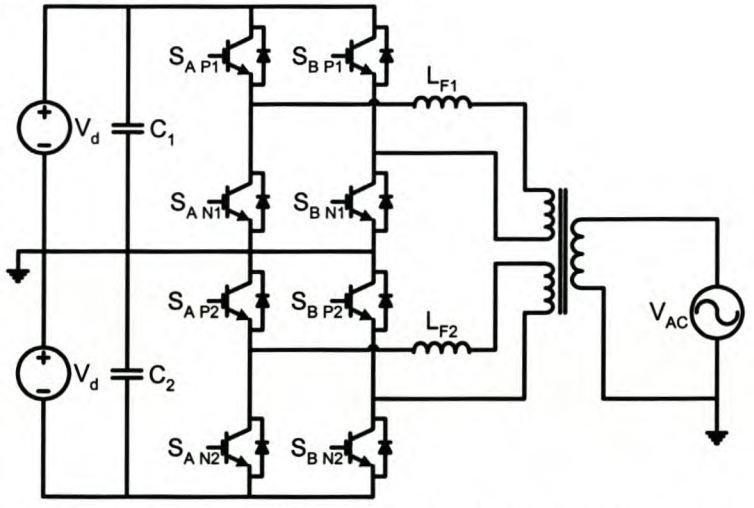


Figure 4-17: The 2-level Series-Stacked Multilevel Converter

The single-phase converter consists of two full-bridge converters stacked on top of each other. Each of the full-bridge units comprises a bus capacitor, four switches and a filter inductor. The topology structure limits the switch voltages to a maximum of half of the total DC bus voltage, with the capacitor dividing circuit helping to maintain this balance. Furthermore, each converter unit switches into isolated windings of a single-phase three-winding transformer. This is a necessary requirement, since it is not possible to connect two different voltage levels to the same load without disastrous consequences. The two converter outputs are recombined in the isolation transformer to produce a single high voltage output, with double the power output level of a single unit, on the load side. The addition of extra voltage levels is easily obtained by simply adding extra half-bridge modules. This does, however, require an isolation transformer with more isolated windings.

4.2.4.2 Waveform Generation

The waveform generation technique for topology is exactly the same as the technique used for explaining unipolar switching in Chapter 2, where switches $S_{A\,P1}$ and $S_{A\,N1}$ are complementary pairs. Each of the converters is sent identical gating pulses, effectively making the two modules of the series-stacked converter operate in parallel. This is the technique shown in Figure 4-18, where the shaded switches represent open switches.

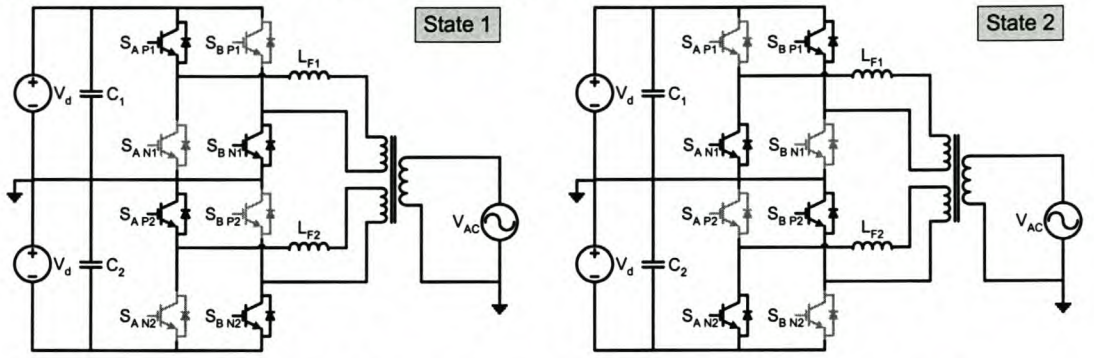


Figure 4-18: Switching States of a 2-level Series-Stacked Multilevel Converter

Unipolar switching facilitates a three-level output voltage waveform, reducing switching harmonics and inductor ratings. The unipolar switching also delivers an output waveform operating at double that of bipolar switching, as can be seen in Figure 4-19.

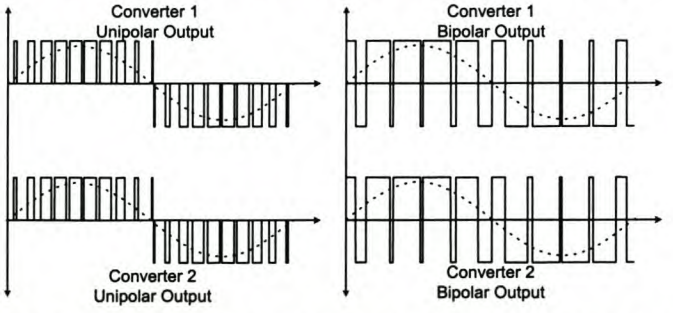


Figure 4-19: Possible Series-Stacked Multilevel Converter Switching Modes

Although illustrating the advantage of unipolar switching, the figure also shows that the converters can be operated using bipolar switching. Yet even in this mode the output voltages, though they are not stepped, are half that of the total DC bus voltage. Both these outputs can further be phase shifted within their switching period, also called interleafing, to further reduce the switching harmonics and increase the apparent switching frequency [70]. The three-level output waveforms of a two-level series-stacked converter, using unipolar switching, are simulated and presented in Figure 4-20. Identical gating pulses are supplied to both converters. With the centre point earthed, Figure 4-17, both outputs are offset to facilitate investigation. The bottom converter's output is offset by –400V, while the top converter's output is offset by 400V.

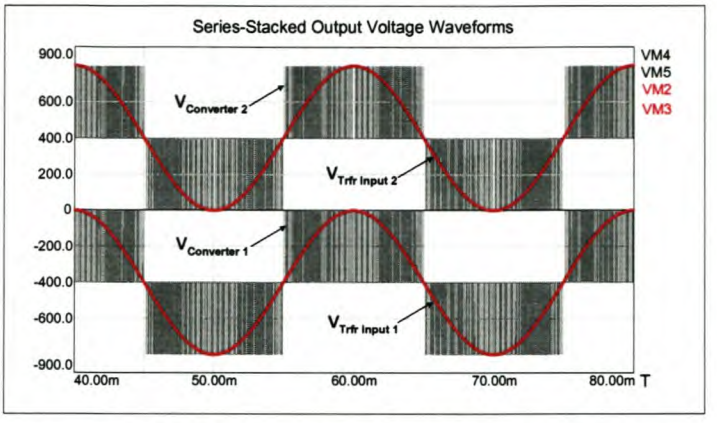


Figure 4-20: Output Voltage Waveforms of a 2-level Series-Stacked Multilevel Converter

4.2.4.3 Topology considerations

4.2.4.3.1 Isolation Transformer

The isolation transformer is the largest disadvantage of this topology, since the transformers are non-standard and this further adds to the cost of the topology. This is, however, not too serious when the converter has to interface with a utility's high voltage levels, since the winding ratios can be increased to interface directly to the power system. The transformer would become fairly large if the application required, for example, an eleven-level converter. This also requires the insulation level to be very high within the transformer. One solution is to possibly use smaller, floating single-phase transformer units, and connect their high voltage terminals in such a manner as to create the multiple-winding isolation transformer.

4.2.4.3.2 Three-Phase Converter Considerations

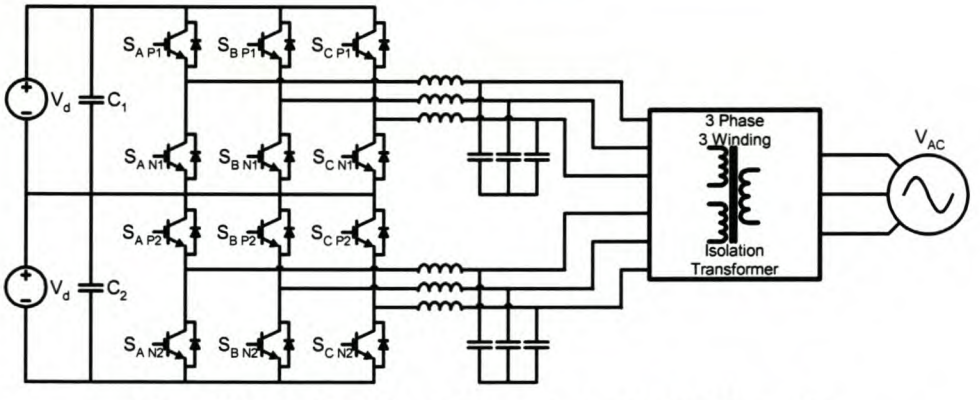


Figure 4-21: A Three-Phase 2-Level Series-Stacked Converter

An advantage of this topology is that the converter can easily be expanded into a three-phase converter by the addition of a single phase-arm to each of the converter levels, and by operating them as coupled three-phase converters, stacked upon each other. Figure 4-21 illustrates the topology layout. The switch component count is the same as that of the other topologies; however, double the number of filter components is required. Added to this is the isolation transformer, increasing the topology's cost. The coupled three-phase converters

make unipolar operation impossible, generating three output states per converter, and thus bi-polar switching is used.

4.2.4.4 Advantages

The advantages are as follows:

- Numerous stepped output voltage levels can easily be created, by the simple addition of converter cells. This has the same effect as creating more stepped voltage output waveforms, since in this topology each level is isolated.
- Simple construction and design.
- Back-to-back operation is possible, sharing the DC bus capacitors.
- Losses within the converter are low as the topology is capable of using various loss reducing switching techniques. The module construction can be optimised for the least circuit losses.
- The single-phase converter can easily be expanded to a three-phase converter, by simply adding one phase-arm, becoming a three-wire coupled converter.
- Phase shifting of the carrier signals further reduces switching harmonics.

4.2.4.5 Disadvantages

The disadvantages are:

- The non-standard isolation and re-combining transformer and its cost.
- In the three-phase mode the three-level stepped output voltage waveform is not available, because of the loss of the zero state.
- High number of filter elements required for the topology.

4.3 Chapter Summary

In conclusion, high voltage solutions were examined and the potential hazards to the converters and equipment were discussed. The various types of multilevel converter topologies were inspected. The topologies and methods of waveform generation of each topology were considered. Special topological considerations specific to each topology were mentioned, and finally advantages and disadvantages of each multilevel converter topology were formulated. Using this information it is possible to make an informed decision as to which multilevel converter topology suits your problem criteria. Solutions can vary from capabilities, component numbers, simplicity or even just topology preference.

4.3.1 Topological Selection

Having analysed the various topologies, their operation and requirements, the Series-Stacked Converter (SSC) and Neutral Point Clamped Converter (NPCC) topologies were chosen as the two topologies of preference. The rest of this thesis is dedicated to the comparison between these two topologies. The primary reasons for choosing these topologies are as fol-

lows:

- Both topologies have the least complicated DC bus requirements. The same DC bus can be used for both topologies, as can be seen in Figure 4-16 and Figure 4-21.
- For comparative purposes, the aim was to construct a single multilevel converter that is capable of being operated in both the SSC and NPCC modes, with the minimum of structural changes. Figure 4-16 and Figure 4-21 show that the SSC and NPCC are the topologies most suited for re-configuration.
- Bi-directional power flow is also easily performed for both topologies, a factor identified when discussing the Traction and MVDC application requirements.
- The additional components required by the SSC and NPCC topologies were easily obtainable.

The primary reasons for not choosing the Flying Capacitor topology, Figure 4-6, were as follows:

- Mentioned in the topological considerations, section 4.2.1.3.2, optimum DC bus capacitor design is complex.
- The topology requires four separate DC bus capacitor limbs, three of which need to be placed as close as possible to the IGBT switches, in order to reduce the parasitic components during switching. The fourth DC bus capacitor limb requires a larger current rating and double the voltage rating of the other capacitor limbs. These conditions do not allow easy re-configuration of the topology.
- The charge-discharge and harmonic elimination control techniques required by the flying capacitor topology, 4.2.1.3.1, was also a deciding factor.

The reasons for not selecting the Cascaded H-Bridge converter topology, Figure 4-11, for the comparison are as follows:

- The topology requires far too many additional components and control to perform bi-directional power flow, requirements of both the Traction and MVDC applications.
- The topology represented in Figure 4-11 requires three isolated DC bus capacitor limbs, being supplied via totally isolated power supplies. Usage of a common DC source is not possible since three-phase switching results in the DC bus being shorted out.
- For a potential MVDC application, back-to-back connection, the H-Bridge converter could suffice; however, maintaining the isolated DC limbs would require each phase to have its own isolated DC power line conductors. The MVDC link, connecting two three-phase networks, requires six separate DC conductors to be strung on the power line.
- The Cascaded H-Bridge topology does not qualify for the re-configuration ability like that of the SSC and NPCC topologies.

The rest of this thesis is subsequently devoted to the operation, control and performance of

the Series Stacked Converter and Neutral Point Clamped Converter topologies.

Chapter 5 Operation and Switching Techniques of the SSC and NPCC

5.1 Overview

In the conclusion of the previous chapter, the SSC and NPCC multilevel topologies were targeted for comparison. This chapter examines the operation and switching techniques, used in this thesis, for both topologies. Increased versatility is also discussed as well as limiting factors. 2-level and 3-level Space Vector Modulation (SVM) is examined. The operation of three-phase 2-level SSC and three-phase 3-level NPCC using SVM is discussed in detail.

Previous chapters discussed inverter and rectifier operation for single-phase converter modules, as well as how these functions are modified to perform various power quality mitigating functions. This chapter does not look at the three-phase SSC and NPCC performing these functions, but does give insight into the converters' operation and the applied switching techniques. The emphasis is on the operational requirements of the two topologies; however, these techniques do provide added insight into the inverting and rectifying modes discussed in chapters 2 and 3.

SVM was selected because the theory can be applied to both topologies. It will be shown that for the NPCC, SVM operation simplifies the switching alternatives for the numerous switching states. Furthermore, SVM offers very good DC bus utilisation for both the SSC and NPCC multilevel topologies. The first of the two chosen topologies to be discussed is the SSC topology. Thereafter the NPCC topology is dealt with. Lastly the potential of implementing a controller, using common SVM techniques applied to both topologies, is discussed.

5.2 The 2-Level Series-Stacked Converter Topology

Illustrated in Figure 5-1 the three-phase SSC topology consists of two three-phase coupled converters that are stacked on top of each other. Each of the converter phase-arms is connected to an electrically isolated winding of a single-phase three-winding transformer. The three isolated transformers are electrically connected via their neutral terminals on both the primary and secondary sides, yielding one large three-phase three-winding transformer. The task of the transformer is to recombine the two sets of three-phase output waveforms that are offset from each by half the full DC bus voltage $2V_d$. The transformer also de-couples the converter stage on the primary side, from the power system on the secondary side, enabling the power system to be grounded in its own required manner, without affecting the converter operation. The primary side transformer connections cause the load to be classed as a coupled load. This means the two series-stacked three-phase converters have to be controlled in the coupled converter mode.

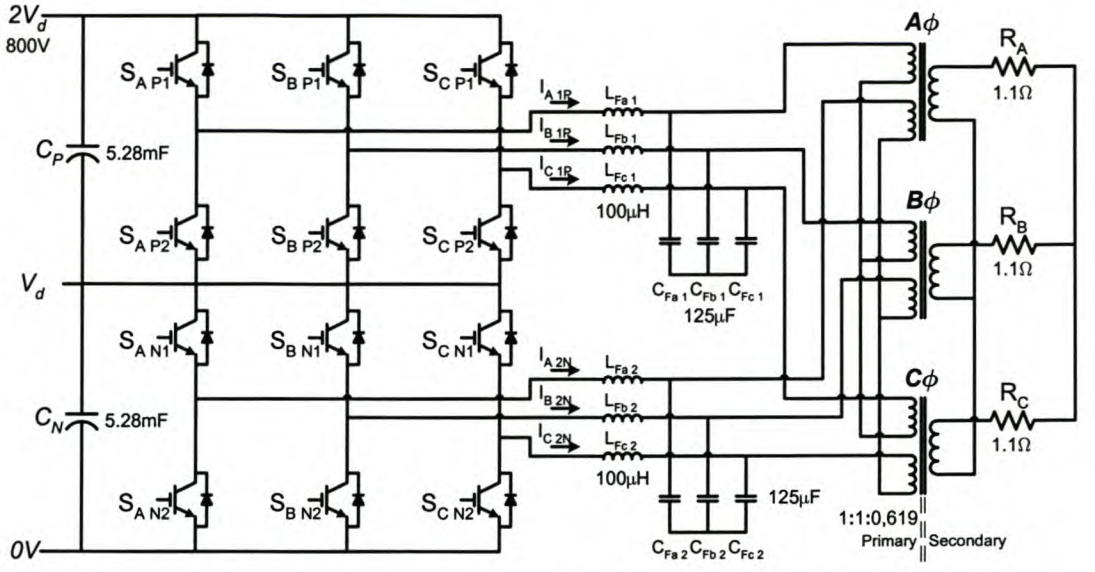


Figure 5-1: The Three-Phase 2-Level Multilevel Converter Topology

The individual three-phase converter modules, the rectifying and inverting modes discussed in chapter 2, require further examination, specifically their switching control requirements during operation. Most of the switching techniques used in chapter 2 applied open-loop modulation to balanced load or loads with returning neutral point connections. However, when the loads are unbalanced, and the same form of open-loop triangle comparison is used on coupled loads, the modulated waveforms look considerably different. In Figure 5-2, one of the two three-phase coupled converter configurations, with the secondary impedance referred to the primary side and connected to an AC source, is shown. During a load imbalance condition, the phases' reflected line impedances differ.

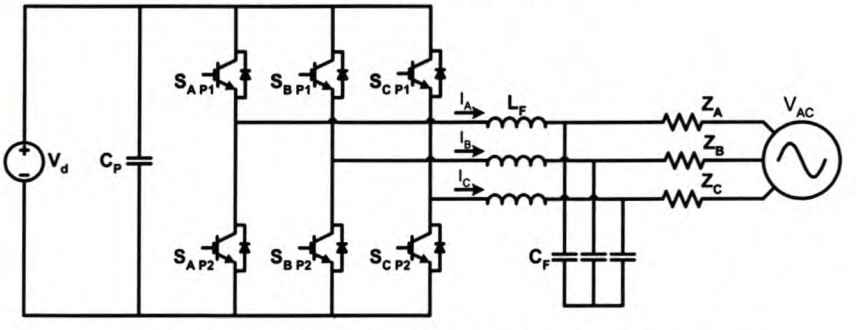


Figure 5-2: Basic 2-Level Three-Phase Coupled Converter

Any attempt at modulating voltage and current waveforms in one phase-arm of a coupled system affects and distorts the waveform modulation in the other two phase-arms. This is because the open-loop modulation, discussed in chapter 2, using the triangular comparison technique, is not capable of compensating for the unbalanced counter Emf. A neutral connection to the centre point of the DC bus is one solution. This creates a return path for the zero sequence currents, reducing the deformation. This is not an option as seen in the transformer connection requirements of Figure 5-1. The phenomenon is deemed a problem even when using closed-loop control, typically predictive current control [72]. Current reference values

become difficult to maintain because of the coupling effect within the three-wire load. This is clearly seen in Figure 5-3, a simulation of this effect.

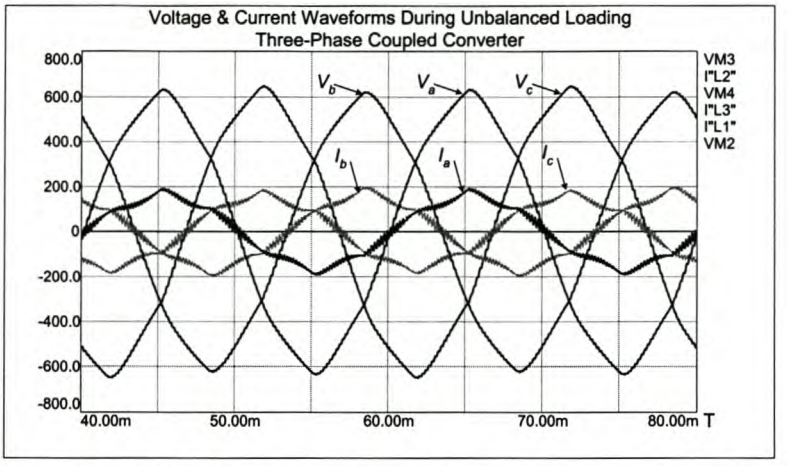


Figure 5-3: Simulated Three-Phase Converter Waveforms - Unbalanced Load

Even though the system voltage, V_{AC}, is sinusoidal and symmetrical, the voltage over the filter capacitors, C_F, is distorted and exhibits the phase imbalance. Phase interaction is thus a factor that impacts largely on the switching control technique. This criterion is used as motivation for the use of the control technique that will be discussed in the next section.

5.2.1 Normal 2-Level Space Vector Modulation Theory

5.2.1.1 General Considerations

SVM is a switching technique typically used to determine the duty cycles of a three-phase converter with a coupled output. Space Vector Modulation provides a technique whereby it is possible to transform the quantities of a three-phase coupled system into a two-phase de-coupled plane known as the α-β plane. Controlling the individual α-β components in the de-coupled plane enables effective modulation of all three phases in a coupled system, insulating the modulation from the coupling effects. However, before dealing with the 2-level SVM there are some important factors to consider and concepts to revise.

The first consideration is that when converting three-phase quantities into a two-phase plane, using some transformation process, the components cannot exclusively be considered as physical voltages and currents. Associating the scalar quantities in the α-β plane as vectors, unnecessary misinterpretation of values is avoided.

Secondly, SVM is a tool used to analyse three-phase coupled networks in a two-phase de-coupled plane. By this is meant that α-plane and β-plane vectors or quantities do not affect each other, i.e. they are de-coupled.

In modulating current and voltage waveforms, positive phase sequence waveforms are usually required when interfacing with existing power networks. To avoid any uncertainty about the transforms used in SVM, it is necessary to revisit the convention of phase rotation. Figure 5-4 is a representation of the conventional phase rotation for a three-phase system of

vectors or phases.

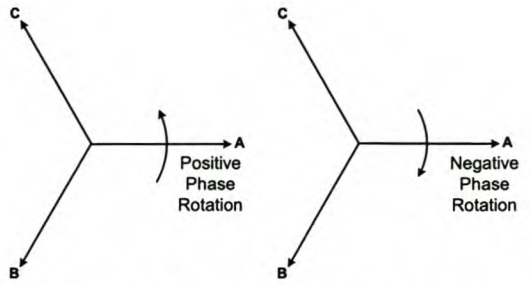


Figure 5-4: Conventional Phase Rotation

Positive phase rotation is defined as the three vectors rotating in an anti-clockwise direction, defining the ABC notation, while negative phase rotation has the vectors rotating in a clockwise direction, thereby generating the ACB phase rotation. Using the convention from Figure 5-4, specifically the phase placement, leads to the interpretation seen in Figure 5-5, when considering the stationary reference frame. Keeping the phase vectors stationary, and only varying them in size from between the vectors' maximum positive and negative values, i.e. zero and ± their peak value with no angular rotation, results in a the phase vector configuration seen in Figure 5-5.

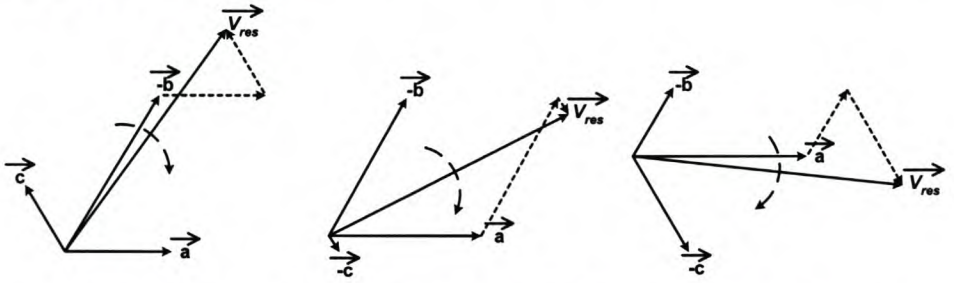


Figure 5-5: Rotation of Resultant Phasor with Negative Phase Placement

Summating the vectors, the resultant vector, V_{res}, is generated. Furthermore this vector rotates in a clockwise direction, indicative of negative phase sequence rotation and not the desired positive phase sequence rotation. The implications of using the phase convention for the stationary reference frame, seen in Figure 5-5, are also seen later in this section.

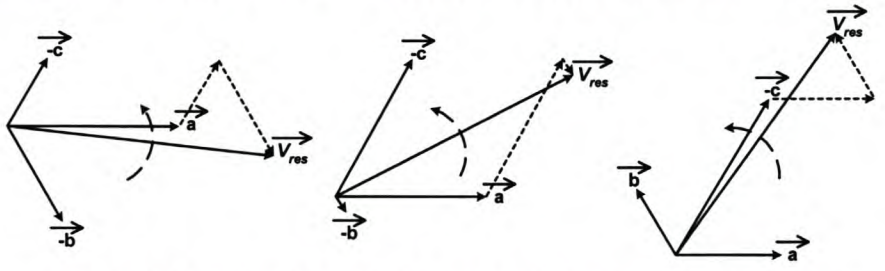


Figure 5-6: Rotation of Resultant Phasor with Positive Phase Placement

Using the convention seen in Figure 5-6, and changing the phase positioning of the B and C phases, a rotating V_{res} is generated, that also rotates in the positive direction. The benefit of using this convention is seen when using the Clarke transform, equation (5.1), or any of the α-β transforms used in the space vector theory.

Using the transform seen in equation (5.1) it is possible to generate the de-coupled α and β vectors from a three-phase coupled system. The zero-vector is defined here for the sole purpose of facilitating the transposing of the matrix [43][45][61][62][63][64][66][68].

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{5.1}$$

This is necessary for determining the three-phase vector magnitudes when working from the α-β plane. Throughout this section, consideration is only given to converters that supply three-wire loads. It is impossible to have zero-sequence currents flowing and therefore the zero-vector in the transformation can be ignored.

The values within the matrix are derived using Figure 5-7. Using each of the phase vectors, equations can be generated for the matrix, to determine the resultant instantaneous vectors that align themselves within the α and β planes.

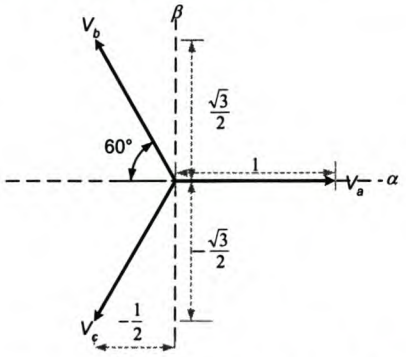


Figure 5-7: Values used in α-β Transformation

With α and β as axis values, the three-phase vectors will increase and decrease, in the same manner as the stationary reference frame in Figure 5-6. The result is a positively rotating reference vector. The fractions in the matrix, used to determine the α-β values, are deduced from standard trigonometric identities. Although the zero-vector is not used, V_0 is derived from using the standard zero-sequence identity (5.2). The ½'s in the matrix are used as a multiplication factor for the $^2/_3$ multiplying factor of the matrix to ensure that equation (5.2) holds true.

$$V_0 = \frac{1}{3}\left(V_a + V_b + V_c\right) \tag{5.2}$$

5.2.1.2 The Normal 2-Level SVM Switching Technique

With the α-β transform identified, the potential switching states of the converter in Figure 5-2 are tabulated in Table 1. Eight possible switching states are obtainable for the standard three-phase converter.

Table 1: A 2-Level Converter's Switching States in Tabular Format

Switching State	Phase		
	A	B	C
0	N	N	N
1	P	N	N
2	P	P	N
3	N	P	N
4	N	P	P
5	N	N	P
6	P	N	P
7	P	P	P

'P' state designations within the phase-arms imply that their top switch, $S_{A\,P1}$, $S_{B\,P1}$ or $S_{C\,P1}$, is closed. If any phase-arm has a switching state of 'N', the phase-arm's switch, $S_{A\,P2}$, $S_{B\,P2}$ or $S_{C\,P2}$, is closed, connecting the load to the *0 V* rail. The switching states of Table 1 are represented graphically in Figure 5-8.

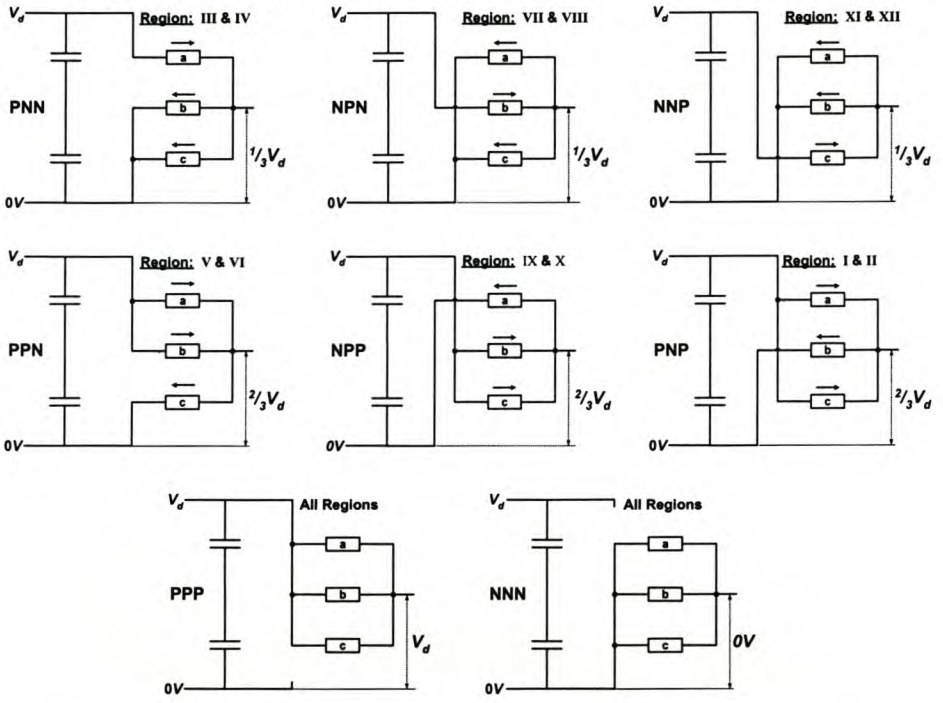


Figure 5-8: Switching States of the 2-Level Converter

The switching states '0' and '7' are referred to as zero states. This is realised when the converter is switched into a PPP or NNN switching state. In any of these states, there is no voltage applied over the filter components and the load, so effectively no current can flow through them, thus the term "zero states". Examining each of the states, Figure 5-8, it is possible to determine in which phases the current is flowing in a positive direction and in which phases the current is flowing in a negative direction, with the positive direction defined as current flowing from the converter towards the star point of the load.

The switching states from Figure 5-8 enable the modulation of the three-phase positive sequence waveforms seen in Figure 5-9. The switching states in Figure 5-8 are also related to periods within the waveforms seen in Figure 5-9. For state PNN, positive current flows in its a-phase while negative current flows in the other two phases. Looking at the waveforms of Figure 5-9, this condition is true in region III and IV, between 60° and 120°, where the a-

phase is positive and the other two phases are negative. This is true for all the switching states, each occurring in their unique region. State PPN occurs in regions V and VI (120° and 180°), state NPN in regions VII and VIII, etc.

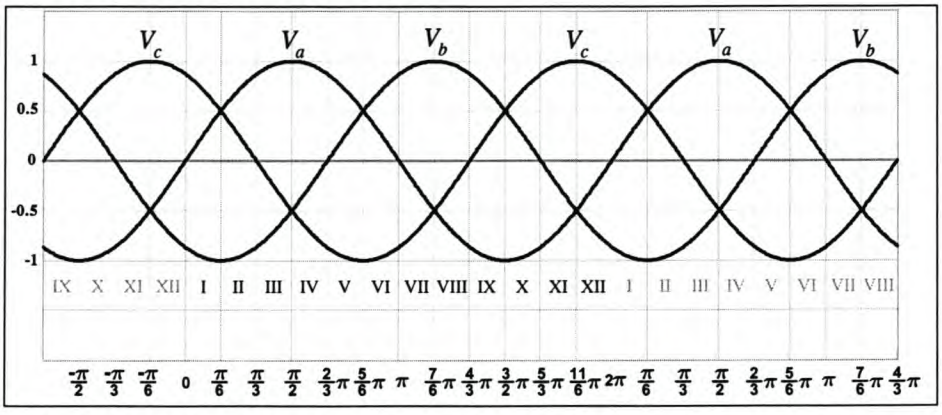


Figure 5-9: Three-Phase Waveforms Positions for Positive Sequence Rotation

Using the three-phase quantities at any point within a region and transforming them into the α-β plane using (5.1) yields a resultant vector for that instant in time. These vectors, the polar representation of the calculated α-β values, are found to be symmetrical around specific axes.

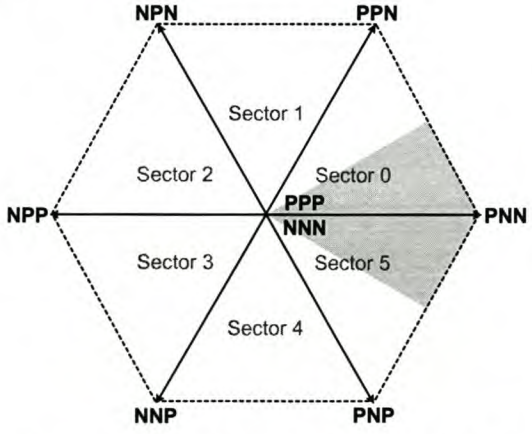


Figure 5-10: State Vectors for 2-Level SVM

Table 2: Summary of Switching States and their Location

Switching State	Phases A-B-C	Operational Sectors	α-β Axis Angle
0	NNN	All	None
1	PNN	5 & 0	0°
2	PPN	0 & 1	60°
3	NPN	1 & 2	120°
4	NPP	2 & 3	180°
5	NNP	3 & 4	240°
6	PNP	4 & 5	300°
7	PPP	All	None

This is best illustrated by an example. State PNN permits operation in regions III and IV in Figure 5-9. These regions are situated symmetrically around the 90° axes. Transforming all the possible three-phase quantities in regions III and IV results in α-β values whose polar vectors lie symmetrically around the 0° axis in the α-β plane. State PNN can thus be plotted as a vector, like that seen in Figure 5-10, situated on the 0° axis. Furthermore the modulation range of state PNN is 30° either side of the 0° axis, indicated as the shaded area in Figure 5-10. The shaded area represents its 60° modulation range [48]. Any polar vector outside the shaded area is that of a different switching state. Similarly all the switching states can be transformed, their α-β axis angles being tabulated in Table 2.

With the knowledge of how the state vectors tie in with the physical three-phase quantities, care should be taken not to forget that the α-β states are vectors and not voltages or currents.

By switching in say state PNN, one generates a vector quantity that effectively grows along the axis represented by PNN. The maximum size of a state vector is determined by considering state PNN, seen in Figure 5-11. With identical resistive loads in each phase and assuming no counter Emf, the voltage at the neutral point can be expected to be $^1/_3V_d$. This means that the phase voltage over the a-phase for state PNN is $^2/_3V_d$, while the voltages over the other two phases are $-^1/_3V_d$.

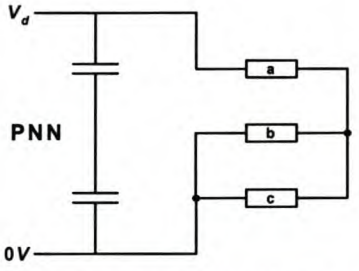


Figure 5-11: Switching State for State PNN

Using these values in the α-β transform (5.1) will yield the following:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} \frac{2V_d}{3} \\ -\frac{V_d}{3} \\ -\frac{V_d}{3} \end{bmatrix}$$

$$\therefore V_\alpha = \frac{2}{3}\left(\frac{2V_d}{3} + \frac{V_d}{6} + \frac{V_d}{6}\right) = \frac{2}{3}\cdot V_d$$

$$\& V_\beta = 0$$

$$\therefore PNN \ \ has \ \ a \ \ length \ \ of = \frac{2}{3}\cdot V_d$$

This implies that the maximum achievable vector length is $^2/_3V_d$. This vector length has nothing to do with the voltages over the load in the three-phase plane. The instantaneous phase voltages sum to V_d, seen in the calculation of V_α above. The state vector size is directly related to the $^2/_3$ multiplier in front of the matrix. This is important when one deals with the instantaneous reactive power theory [43], which uses a $^{\sqrt{2}}/_{\sqrt{3}}$ multiplying factor. Using the transform in [43], the $^{\sqrt{2}}/_{\sqrt{3}}$ factor influences the length of the state vectors. In summary, the size of the state vector is dependent on the size of the DC bus and the transformation factor used with the matrix. As mentioned, this factor does differ with different transforms [43][62][65].

With the origin of the α-β vector values obtained, and because of how the various switching states correlate with the switching vectors in the α-β plane, it is necessary to consider how the duty cycles are calculated using SVM. Normally a converter uses a control system that provides the controller with a reference value that the controller needs to achieve. For 2-level SVM this reference is generated in the de-coupled α-β plane. The measured three-phase quantities on the converter output are transformed into α-β plane. The difference between the

two quantities is what the controller uses to calculate the duty cycles, in order to minimise the difference. Without focussing on the control strategy, it is possible to analyse how the duty cycles are generated just using the α-β vector reference values.

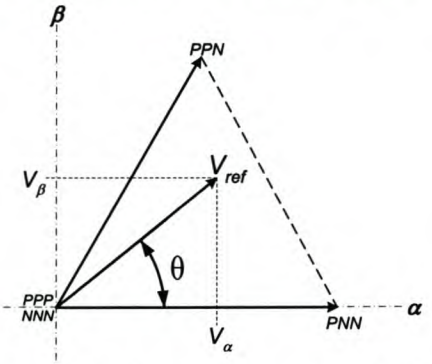


Figure 5-12: State Vectors within Sector 0, for 2-Level SVM

Figure 5-12 shows how the V_α and V_β vectors' values sum up to form V_{ref}, a vector with an angle, denoted as θ, that for this explanation lies in Sector 0. Using all four switching states available to Sector 0, the vector V_{ref} is generated. To reduce the switching harmonics, only one switch is switched at a time. Using the 2 zero states, in conjunction with symmetrical PWM, results in a switching sequence as follows: NNN → PNN → PPN → PPP → PPN → PNN → NNN, as seen in Figure 5-13.

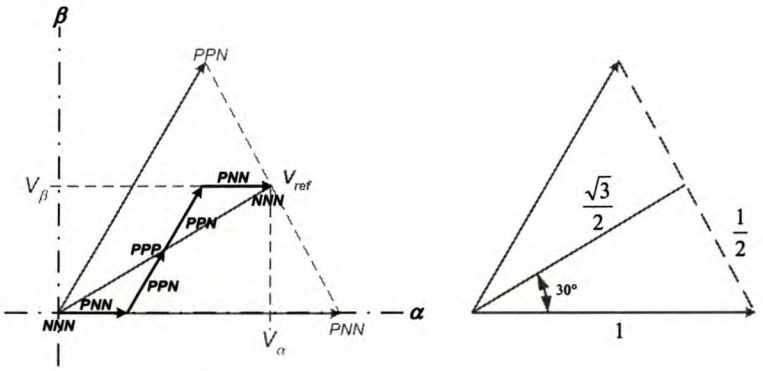


Figure 5-13: Symmetrical PWM Functionality and Vector Lengths

The length of the vector V_{ref} is also an important consideration. Any V_{ref} with a magnitude exceeding the dotted boundary line connecting the state vectors PNN and PPN cannot be generated. A V_{ref} longer than this line would result in the converter going into over-modulation, because the switching states cannot be utilised for longer in the switching period. The identity triangle on the right in Figure 5-13 also shows what the maximum amplitude of the modulated three-phase voltages can be before the converter goes into over-modulation. If the length of PNN is assumed to be unity, ignoring the multiplying factor and DC bus value discussed previously, the length of the vector V_{ref} cannot exceed $\sqrt{3}/2$. Thus identity (5.3) is deduced.

$$V_{ref} = m_a \cdot \frac{\sqrt{3}}{2} \cdot V_d \tag{5.3}$$

With V_{ref} being limited to $\sqrt{3}/2$ p.u., a boundary limit can be superimposed on the switching

state diagram to indicate its limit of operation, seen in Figure 5-10. It is also possible to obtain V_{ref} using the polar format seen in (5.4)

$$V_{ref} = \frac{2}{3}\left(V_a + V_b \times e^{j\cdot\frac{2\pi}{3}} + V_c \cdot e^{j\cdot\frac{4\pi}{3}} \right) \tag{5.4}$$

Using the identity (5.3) the reference value can be expressed as (5.5) in its polar form.

$$V_{ref} = m_a \cdot \frac{V_d}{\sqrt{3}} \cdot e^{j\cdot\theta} \tag{5.5}$$

Expressing the reference value with respect to an angle, θ, and a modulation index, m_a, increases the versatility of the equation. Using these two values, the duty cycles for the various switching states can be calculated. There are various techniques in determining these duty cycles [76][77][78]; however, using m_a and θ enables duty cycles to be generated from various types of control techniques. This facilitates the simplification of the duty cycle equations, where one set of formulas can be used for all the sectors, unlike the above referenced methods. Using p.u. values in conjunction with m_a and θ simplifies the task of calculation and allows movement through the transform without any changes in their values occurring.

5.2.1.2.1 Duty Cycle Calculations for Normal SVM

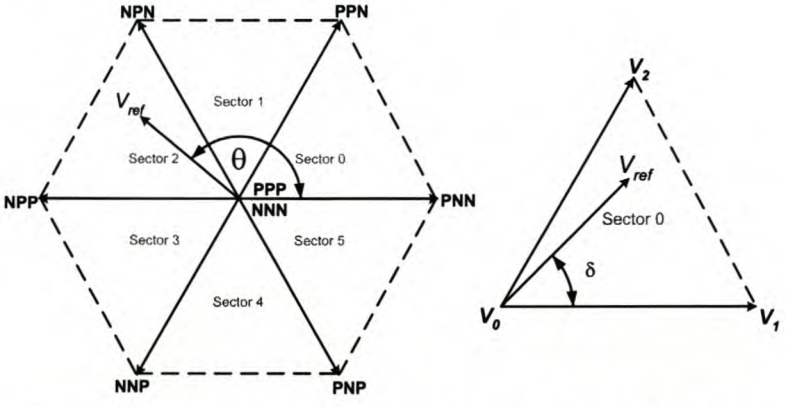


Figure 5-14: Referring the Reference Vector back to Sector 0 for 2-Level SVM

The first objective is to determine in which sector V_{ref} lies, so that it is possible to determine which switching state vectors need to be used. Thereafter the calculation of the required duty cycles of the switching states, used to generate V_{ref}, is performed. Looking at Figure 5-14, the state vectors, a circular symmetry is noticed. A reference voltage has also been superimposed onto the switching states. The vector V_{ref} is expressed with respect to m_a and its associated angle θ. The circular symmetry allows the vector to be rotated back into the first sector, sector 0. The angle θ is redefined as angle δ, while the absolute value of V_{ref} remains unchanged. The first sector can now be used to calculate the duty cycles for all the sectors in which the reference vector occurs. Vectors V_1, V_2 and V_0, seen surrounding sector 0, represent the state vectors of the relevant sector, while the relevant duty cycles are represented as D_1, D_2 and D_0. Identity (5.6) defines that the sum of the three duty cycles should not exceed one switching period; this also coincides with the discussion on the prevention of over-

modulation.

$$D_1 + D_2 + D_0 = 1 \tag{5.6}$$

The polar forms of the vectors V_1, V_2 and V_0 are determined and are as follows:

$$V_1 = 1 \quad AND \quad V_2 = 1 \cdot e^{j\frac{\pi}{3}} \quad AND \quad V_0 = 0 \quad AND \quad V_{ref} = V \cdot e^{j\delta} \tag{5.7}$$

Unity switching state vectors are used, in accordance with the identity used in (5.5). Using the principle of symmetrical PWM switching, shown in Figure 5-13, equation (5.8) is derived.

$$V_1 \cdot D_1 + V_2 \cdot D_2 + V_0 \cdot D_0 = V \cdot e^{j\delta} \tag{5.8}$$

Substituting (5.7) into (5.8) obtains the following:

$$D_1 \cdot 1 + D_2 \cdot \left(\cos\frac{\pi}{3} + j \cdot \sin\frac{\pi}{3} \right) = V_{ref} \left(\cos\delta + j \cdot \sin\delta \right) \tag{5.9}$$

(5.9) is then separated into the real and imaginary components to obtain the following:

$$\text{Re}: D_1 + D_2 \cdot \cos\frac{\pi}{3} = V_{ref} \cdot \cos\delta$$

$$\text{Im}: D_2 \cdot \sin\frac{\pi}{3} = V_{ref} \cdot \sin\delta$$

Using trigonometric substitution:

$$\text{Re}: D_1 + D_2 \cdot \frac{1}{2} = V_{ref} \cdot \cos\delta$$

$$\text{Im}: D_2 \cdot \frac{\sqrt{3}}{2} = V_{ref} \cdot \sin\delta$$

Representing this in matrix format yields the following:

$$\begin{bmatrix} 1 & 1 & 1 \\ 1 & \frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & 0 \end{bmatrix} \cdot \begin{bmatrix} D_1 \\ D_2 \\ D_0 \end{bmatrix} = \begin{bmatrix} 1 \\ V_{ref} \cdot \cos\delta \\ V_{ref} \cdot \sin\delta \end{bmatrix}$$

From these results and using identity (5.3), where V_d is the unity value, it is possible to derive the following equations:

$$D_2 = m_a \cdot \sin\delta \tag{5.10}$$

$$D_1 = m_a \cdot \sin\left(\frac{\pi}{3} - \delta \right) \tag{5.11}$$

$$D_0 = 1 - (D_1 + D_2) \tag{5.12}$$

These equations simplify the control algorithms of the controller, reducing the need for duty cycle calculations in each sector, and freeing up processor resources. With the duty cycles calculated, the switching times can be applied to the switching state vectors surrounding the sector in which V_{ref} is located. Using Figure 5-14 as an example, the reference in sector 2 can be modulated by switching the converter into state NPN for the period D_1, state NPP for the period D_2 and states PPP and NNN for the period D_0. These states are typically applied using the symmetrical PWM shown in Figure 5-13.

Further proof of the SVM technique having a higher DC bus utilisation can be seen when examining Figure 5-15.

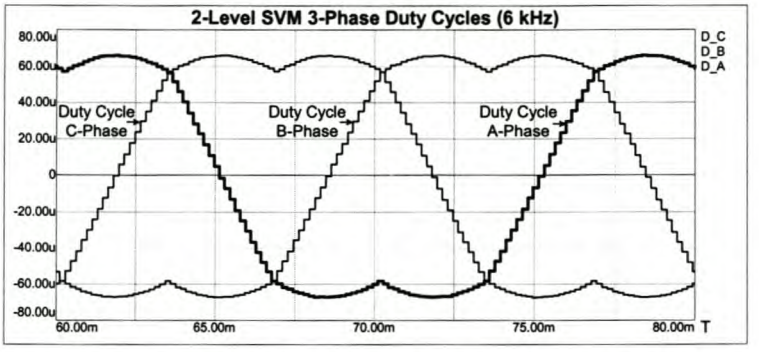


Figure 5-15: Typical SVM Duty Cycle Modulation Functions

The figure illustrates the duty cycle modulation functions for each phase-arm when trying to modulate three-phase waveforms. Each waveform is representative of the times that each individual phase-arm is switched. The benefits of SVM modulation are seen in comparing these waveforms to the duty cycle modulation function of open-loop sinusoidal PWM in Chapter 2. Three-phase duty cycle functions, when using sinusoidal PWM, yield three sinusoidal waveforms with no flattening on their peaks. The flattened peaks of the SVM modulation permit larger output voltages to be modulated, hence better DC bus utilisation [65].

5.2.1.3 DC Bus Unbalance Concerns SSC (Normal SVM)

A significant concern when implementing a multilevel converter is the balancing of the DC bus capacitors. Unbalance between the capacitors can originate from various conditions, typically system transients, large load steps and component imperfections. During these conditions, the voltage sharing between the capacitors is uneven. This can lead to switch destruction if the unbalance becomes too large.

However, analysis has proved that the internal losses within the converter unit lead to self-balancing of the DC bus capacitors [54]. In other words, the unbalance oscillations seen on the DC bus are damped by the resistive elements within the converter. It was also found that significant reductions in DC bus oscillations are achieved if the capacitor ratings are designed according to (5.13) [54].

$$C_P \geq \frac{1}{L_F \omega^2 \pi^2} \tag{5.13}$$

Where L_F is the filter inductor and ω is the angular switching frequency. Using (5.13), a minimum DC bus capacitance of 1.1 mF is required to enhance the stability. For the SSC used in the simulation, the DC bus capacitance was 5.28 mF, thus stable operation was obtained.

5.2.1.4 Normal SVM Implementation on the 2-Level Series-Stacked Converter

As mentioned in the beginning of this chapter, the SSC can be switched using various alternative switching techniques; however, the SVM technique was selected for the comparative study between the two converter control techniques. Re-examining the SSC topology, Figure 5-16, shows that the converter uses 12 switches, six for each of the individual three-phase

converters stacked upon each other. The SSC structure and capacitors C_P and C_N ensure that the switch voltages are not exceeded [10][70]. Using the previously discussed theoretical derivations for SVM, both converters are switched using the same duty cycles. This technique will be referred to as normal SVM for the 2-level converter. Sending identical pulses to both the top and bottom converters results in two individual sets of three-phase sinusoidal waveforms being generated. Both sets of three-phase waveforms are then recombined in the isolation transformer, as discussed in Chapter 4 under the heading Waveform Generation.

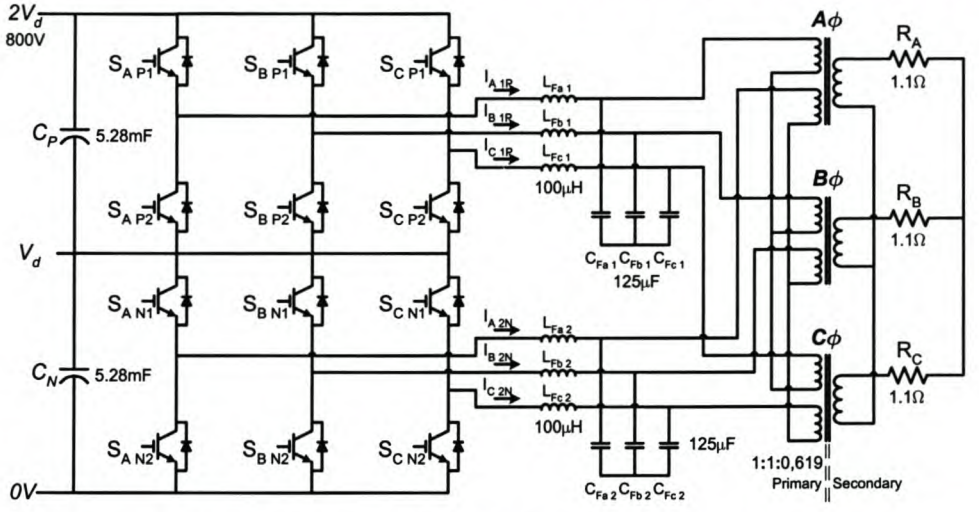


Figure 5-16: The 2-Level Series-Stacked Converter

Open-loop SVM simulations on the 2-level SSC are implemented using SIMPLORER®, the simulation model, details listed in Appendix A. Defining the reference vector, V_{ref}, in terms of the modulation index, m_a, requires p.u. values to be used. This simplifies the calculations. V_{ref} is then rotated through 360°, with step sizes, θ, equal to the switching frequency divided by the fundamental frequency.

The simulated output voltage waveforms, on the secondary side of the transformer, of the SSC converter model can be seen in Figure 5-17. The multilevel converter parameters for the simulation are listed in Table 3. From the results it is possible to determine that the equations derived for the open-loop control of the 2-level series-stacked converter modulate satisfactory load voltage waveforms with minimal distortion.

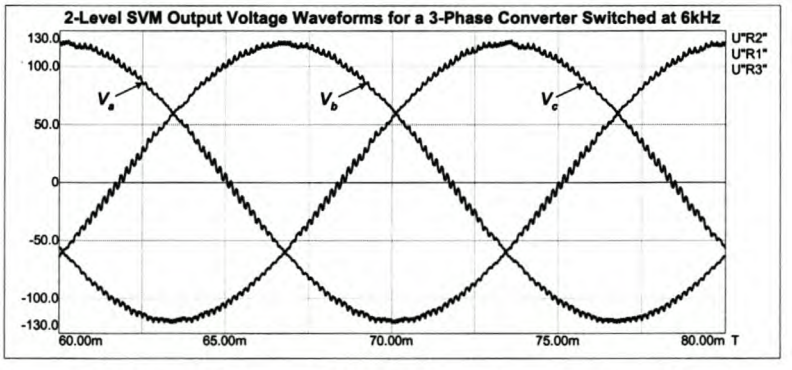


Figure 5-17: 2-Level Normal SVM 3-Phase Output Voltage Waveforms

Table 3: SSC Simulation Parameters Using Normal SVM

Components	Values
DC Bus	840 V
Switches	Ideal
Filter Inductors	100 μH
Filter Capacitors	125 μF
DC Bus Capacitance	5.28 mF
Transformer Ratios	1: 0.619
Load Resistance	1.1 Ω
Switching Parameters	
Modulation Index	0.8
Switching Frequency	6 kHz

5.2.2 Interleaved 2-Level Space Vector Modulation Theory

5.2.2.1 The Interleaved Switching Technique

Interleaved switching, first developed for converters operating in parallel [49], is a switching technique that is used for increasing the effective switching frequency of multiple converters operating as a single unit. The technique is ideally suited for series-stacked converters. Switches at different levels are isolated from each other by the series-connected bus capacitors, clamping the DC bus voltages [50][52]. Increasing the effective switching frequency of the converter results in an output waveform with reduced harmonics.

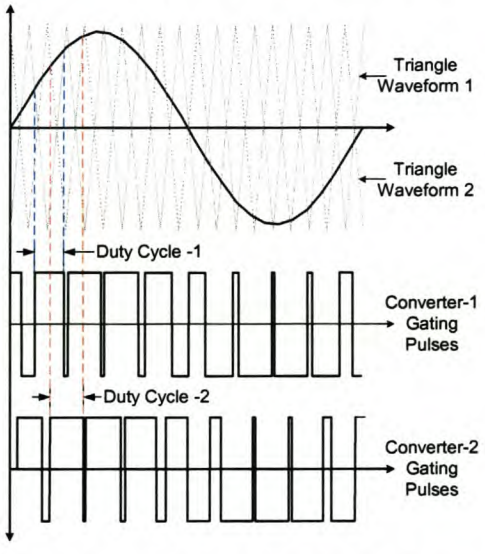


Figure 5-18: Interleaved Switching Concept

The increased effective switching frequency causes the harmonics to appear at higher frequencies [10][49][50][51][52][53][54], i.e. multiples of the effective switching frequency. The technique is best described by analysing a single-phase example using open-loop SPWM, like that seen in Figure 5-18.

Implementation of this technique involves the phase shifting of the triangular carrier waveforms. The number of carrier waveforms used is typically equal to the number of series-stacked converter modules. The phase shifting of the carrier waveforms results in a slight staggering of the gating pulses sent to the same phase-arms of the top and bottom converters,

creating the overall effect of increased switching frequency.

The magnitude of the required phase shift is determined by the following equation:

$$\theta_{shift} = \frac{n \times 2\pi \times f_{fund}}{N \times f_{Carrier}} (rads) \tag{5.14}$$

$$Where: n = cell\ number\ (n = 0,1,2..,N-1)$$

$$N = number\ of\ cells$$

In Figure 5-18, the effect of the phase-shifted carrier can be observed. Delaying the gating pulses of the second converter for half a switching period results in the reference waveform becoming larger. The changing reference waveform results in a gating pulse with a longer duty cycle being sent to the second converter. This property is inherently common to all forms of interleafing, regardless of the switching scheme or number of converter levels.

Interleafing of 2-level SVM is performed by calculating the duty cycles in the same manner as that of the normal 2-level SVM technique. The variation is that the gating pulses for one of the converters in the 2-level SSC are implemented half a switching period later than that for the other converter. As expected, the duty cycles will differ slightly, due to the delay in calculation time, by which time V_{ref} has advanced slightly [70]. The two outputs are once again combined in the isolation transformer, effectively doubling the switching frequency of the SSC and resulting in an output waveform with a reduced switching ripple. The effect of the phase shifting using SVM can be seen when considering the duty cycle modulation function seen in Figure 5-19.

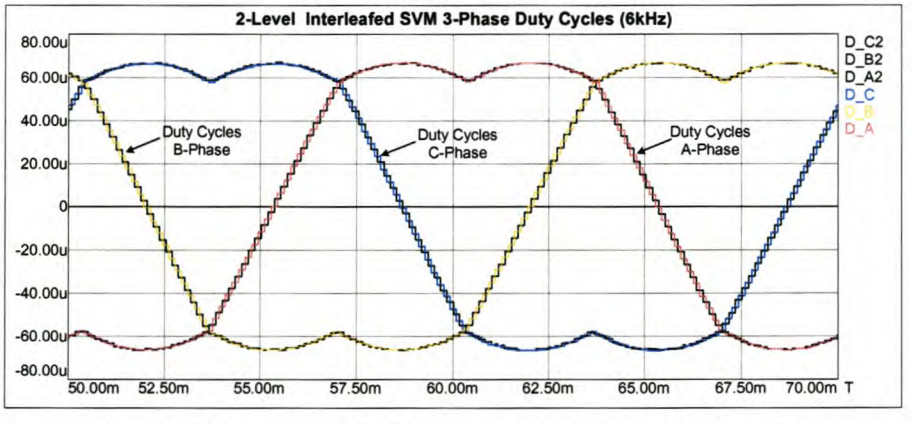


Figure 5-19: Interleaved SVM Duty Cycle Modulation Functions

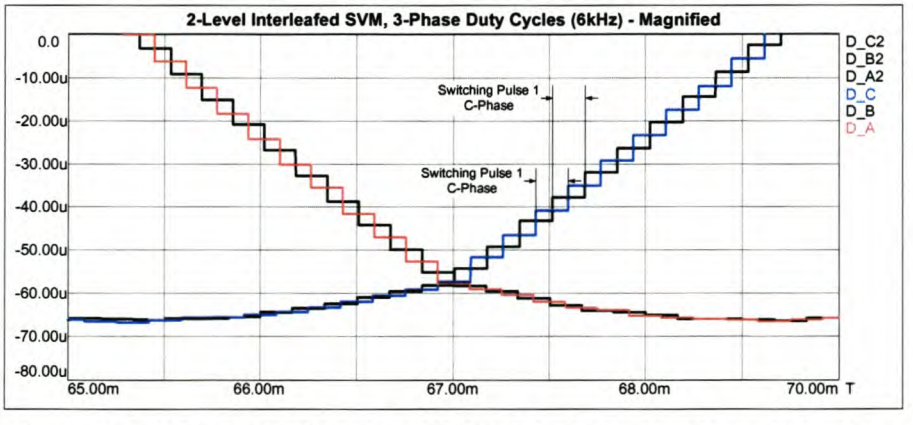


Figure 5-20: Interleaved SVM Duty Cycle Modulation Functions – Magnified

It is more apparent when considering the magnified portion of Figure 5-19 in Figure 5-20. Because of the flat peak nature of the SVM modulation function, the interleafing effect is better observed on the rising and falling edges of the waveform.

5.2.2.2 DC Bus Unbalance Concerns SSC (Interleaved SVM)

The SSC using interleaved SVM is vulnerable to the same unbalance conditions discussed for the SSC using normal SVM. However, a second unbalance mechanism, associated with the switching harmonics, occurs while using interleaved switching [54]. Further investigation into this mechanism has shown that the load impedance also plays a role in the unbalance mechanism. Balancing is thus achieved provided that the load current does not contain harmonics near twice the switching frequency and multiples thereof. Therefore the switching frequency chosen is required to be significantly higher than the highest frequency component of the reference signal and load current. Ensuring these parameters results in the SSC, using interleaved SVM, rebalancing faster than the SSC using normal SVM. Studies have shown that this is due to the increased energy loss in the bus and load resistance as a result of the second balancing mechanism [54].

5.2.2.3 Interleaved SVM Switching Implementation on the 2-Level Series-Stacked Converter

The SVM switching technique, described in section 5.2.1.2, has been implemented in SIMPLORER® with the phase shifting technique, calculated according to (5.14), in order to simulate the interleafing of the SSC. Two separate reference detectors are used to calculate the duty cycles and sent to the appropriate switches. The model is listed in Appendix A.

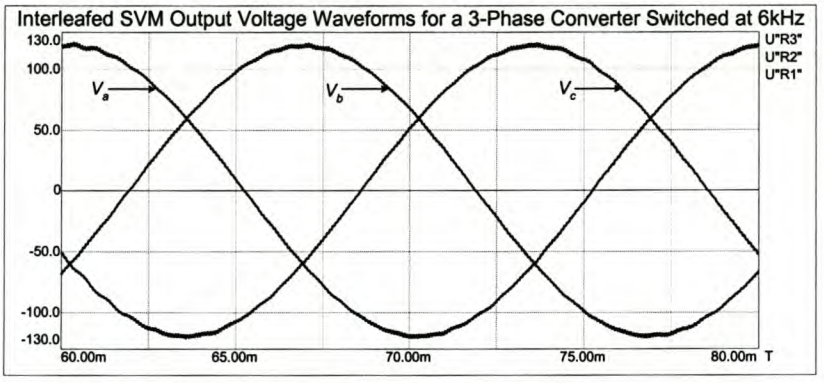


Figure 5-21: 2-Level Normal SVM 3-Phase Output Voltage Waveforms

Using the exact same simulation parameters as stated in Table 3 and the model seen in Figure 5-16, the simulation generated the load side voltage waveforms seen in Figure 5-21. The simulated interleaved switching model yields voltage waveforms with considerably less voltage harmonics, as expected from the theory [10][49][50][51][52][53][54], than the switched waveforms of the normal SVM switching scheme, seen in Figure 5-17. Further analysis of the interleaved SVM switching performance will be discussed in the next chapter.

5.3 The 3-Level Neutral Point Clamped Converter Topology

Basic operation of the NPCC, dealt with in Chapter 3 and displayed in Figure 5-22, highlighted that this multilevel converter topology is capable of waveform modulation using three output voltage levels, while operating at twice the normal converter DC bus voltage. These capabilities are made possible by the combined operation of the converter's freewheeling diodes, D_1 to D_6, and their connection to the capacitors C_P and C_N, while modulating an output waveform. Each switch is thus only exposed to a maximum voltage of $\frac{1}{2}V_d$. The complementary switching pairs are $S_{X\,P1}$-$S_{X\,N1}$ and $S_{X\,N2}$-$S_{X\,P2}$, where x denotes the relevant phase. The three output voltage levels also result in the reduction of the ripple current flowing through the filter inductors, making it possible to reduce their required ratings.

Figure 5-22 also shows the converter connected to a three-phase, three-winding transformer. This is not necessary as the NPCC can be connected directly to the network; however, for comparative purposes and to ensure that both topologies have the same loading conditions, the transformer is inserted. Furthermore, the isolation between the AC network, on the secondary side, and the converter makes it possible to operate using two different earthing strategies, and thus the centre point, denoted *N* in Figure 5-22, need not be earthed. More detail on the effect of the transformer and its impact on the filter components is dealt with in the next chapter.

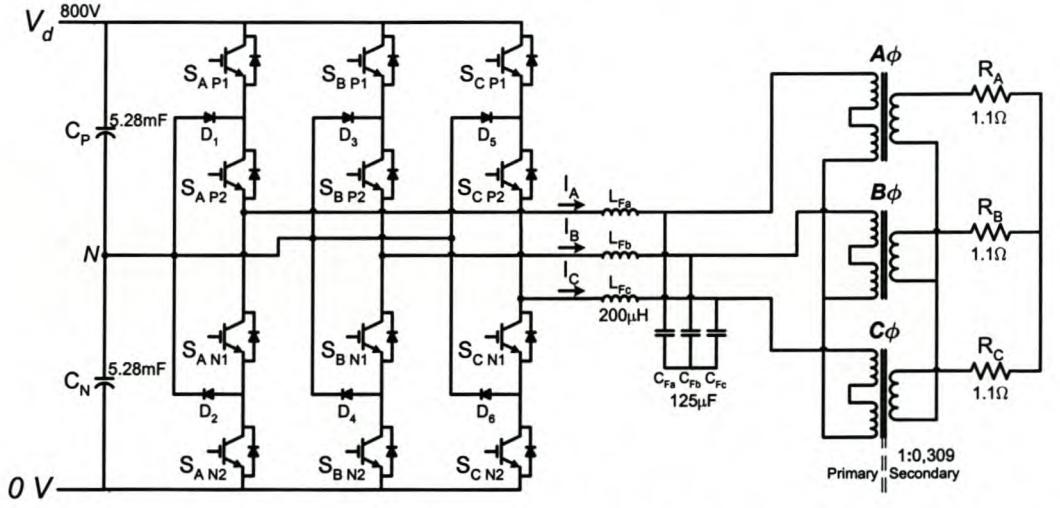


Figure 5-22: The 3-Level NPCC

A NPCC disadvantage is the increase in component count, due to the diodes. However, even though the diodes are associated with extra parasitic components and losses, their cost is considerably less than the injection transformer and extra filter components seen in the SSC topology. This transformer-less solution is seen as a major benefit of the topology, especially if more than three levels are required

5.3.1 The 3-Level SVM Switching Technique

Switching of the 3-level NPCC topology requires a somewhat different approach to the

switching approach discussed in Chapter 4. The effects of switching in an open-loop unipolar method prove to be problematic when considering the three-phase model. Interaction between the phases occurs and complicates the switching technique. This is one of the reasons why 3-level SVM is considered. Operation in the α-β plane, a previously mentioned property of the transformation, facilitates the controlling of three-phase quantities without the phase interaction playing a part.

For the 3-phase NPCC to be able to generate three output voltage levels per phase namely V_d, $\frac{1}{2}V_d$ and *0 V*, the switches have to be switched in such a manner as to connect the centre point of the converter, *N* in Figure 5-22, to the load. This is achieved, in a single phase-arm, by closing switches S_{XP2} and S_{XN1} while switches S_{XP1} and S_{XN2} are kept open, where *x* is either phase A, B or C. The effect of this is that the driving voltage onto the specific phase load, on the converter side, becomes $\frac{1}{2}V_d$. Earthing the converter on the centre point results in a converter side phase driving voltage of *0 V*, hence it being called a zero state. Throughout this thesis, when switches S_{XP2} and S_{XN1} are closed, it will be referred to as a zero state. All the per-phase switching state options are listed in Table 4.

Table 4: Possible Switching States for the A-Phase of a NPC Converter

Switching State	Switch			
	S_{XP1}	S_{XP2}	S_{XN1}	S_{XN2}
P	ON	ON	OFF	OFF
O	OFF	ON	ON	OFF
N	OFF	OFF	ON	ON

The suffixes 'P' and 'N' imply that the outputs of each of the phases are either connected to the positive rail 'P', or the negative rail 'N', or in the case of Figure 5-22 the 0 V rail. Switching the zero state, '0', permits the freewheeling currents to flow via diodes D_1 to D_6, depending on the current direction. Important to note is that while switching a 'P' state in one phase-arm, the current return path can be through the zero state in one of the other two phase-arms. So in the three-phase converter topology, freewheeling currents flowing between phases does not affect the bus capacitors, unlike the case in a single-phase converter, where the only path is through the DC bus capacitors.

Furthermore, when measuring switching voltages between two phases, it is observed that the converter is capable of generating five output voltage levels between phases, like those seen in Figure 5-23.

Using the single-phase states from Table 4 and applying them to a three-phase system, a typical three-phase switching state would be PNO. This convention applies to each phase-arm in the order A, B and C. Thus 27 different switching permutations for the three-phase converter are available, as opposed to the 8 different states used for 2-level SVM. This high number of switching states makes it necessary to revise the SVM switching technique. Although the basis of the SVM theory remains the same, the extra switching states enable the

generation of extra switching vectors.

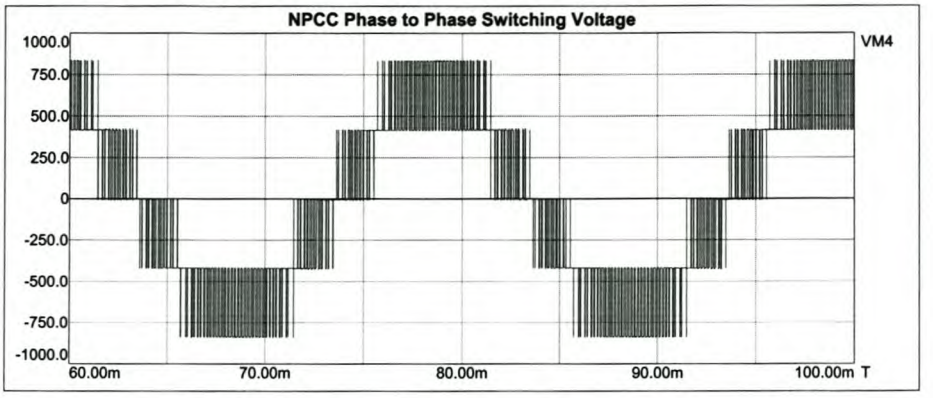


Figure 5-23: Three-Phase NPCC Phase-Phase Switching Voltage

Using these 27 switching states, it is possible to subdivide the vectors generated into four groups. These are named the large, medium, small and zero state vectors as seen in Table 5.

Table 5: Various Switching State Vectors for 3-Level SVM applied to a NPC Converter

Large Voltage Vectors	Medium Voltage Vectors	Upper Small Voltage Vectors	Lower Small Voltage Vectors
PNN	PON	POO	ONN
PPN	OPN	PPO	OON
NPN	NPO	OPO	NON
NPP	NOP	OPP	NOO
NNP	ONP	OOP	NNO
PNP	PNO	POP	ONO

The grouping will become apparent once the state switching vectors are discussed. The zero state vectors are omitted from Table 5 and are simply PPP, OOO and NNN. The small voltage vectors are further subdivided as upper and lower voltage vectors, depending on which half of the DC bus they are connected to in that state.

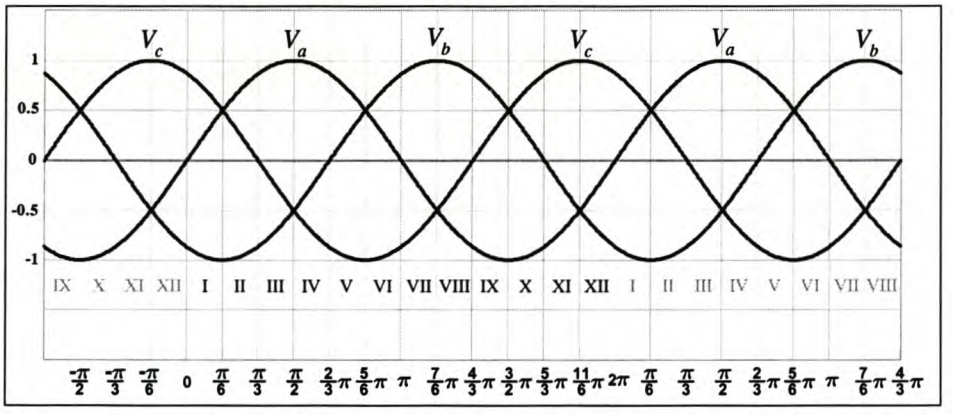


Figure 5-24 Three-Phase Waveforms Positions used for 3-Level Explanation

In order to verify the positioning of the switching state vectors in the α-β plane, it is once again necessary to look at a set of three-phase waveforms that one aims to generate using SVM, as seen in Figure 5-24. Looking at the large voltage vectors, identified in Table 5, it is possible to obtain these switching states in the manner seen in Figure 5-25. These large voltage vectors are identical to those seen in the 2-level SVM. Using Figure 5-24, the regions of the various switching states in the three-phase plane can be determined.

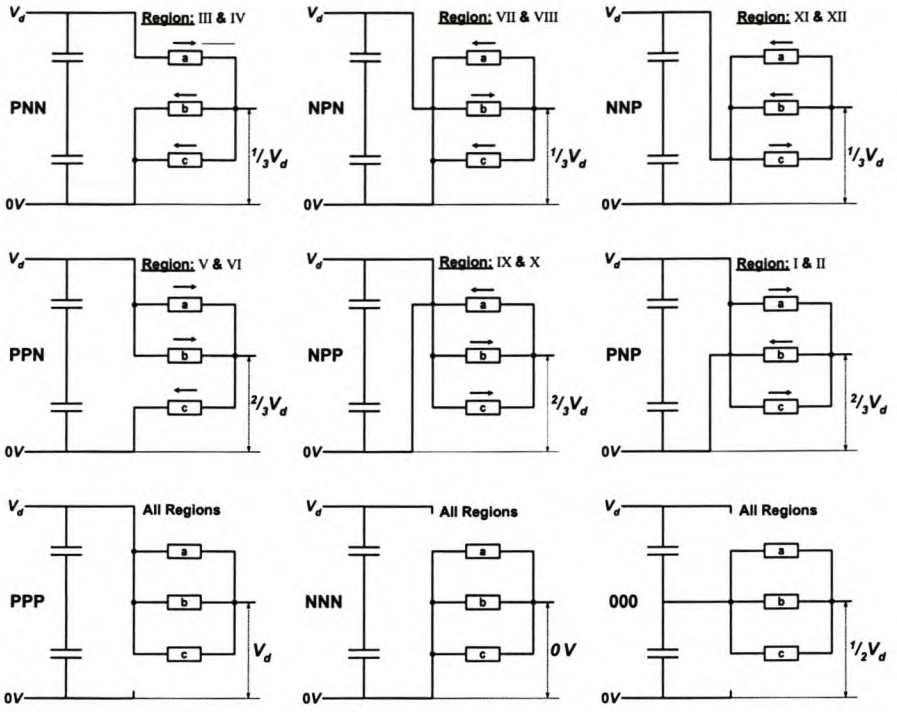


Figure 5-25: Large Voltage Switching States of the 3-Level Converter

By this is meant that for the switching states PNN, for example, the potential waveforms that can be modulated lie in regions III and IV.

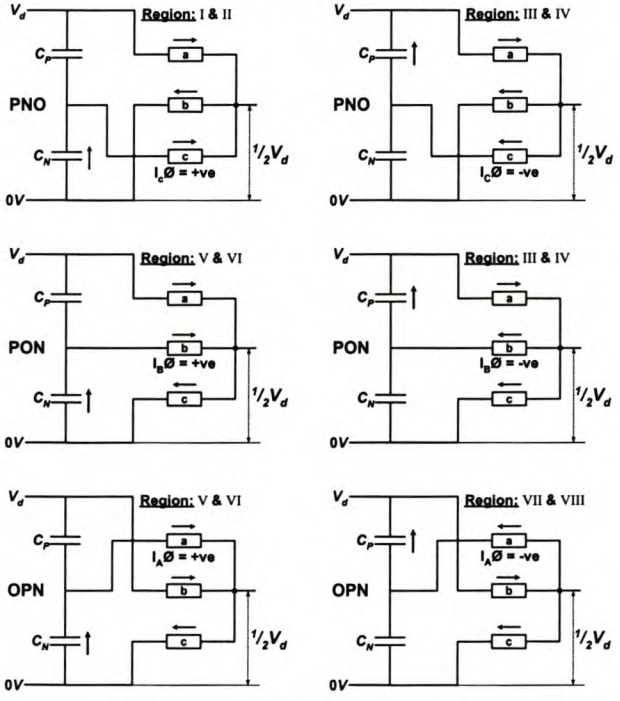


Figure 5-26: Medium Voltage Switching States of the 3-Level Converter, States PNO, PON & OPN

The voltages on the star point of the loads are also considered. The maximum voltage achievable over a single phase-arm's load is $^2/_3V_d$. This must not be confused with the multiplying factor associated with the α-β transform; it is merely to show that this state subjects one of the phases to the largest DC bus value. Using Figure 5-25 it is possible to identify all the regions in Figure 5-24 in which these states occur. This information is used later when

generating the vector diagram of the switching vectors in the α-β plane.

The next set of vectors shown in Table 5 were the medium voltage vectors. There are a total of six switching states and these can be seen in Figure 5-26 and Figure 5-27. Looking at Figure 5-26, the medium voltage vector PNO is shown twice. The reason is that state PNO can have current flowing in both directions in the C-phase. This implies that the switching state can be used for modulation in regions I, II, III and IV in Figure 5-24, depending on the current direction.

A second observation is that this state can draw energy from either capacitor C_P or capacitor C_N in the DC bus, also depending on the current direction. It is this switching state that makes the centre point unstable, especially during transient disturbances. The reason for the neutral point imbalance is the constant drainage of energy from one half of the DC bus for the duration of two switching regions, seen in Figure 5-24 and in Figure 5-26. However, during steady state conditions, the average charge/discharge energy through the capacitors is zero over a fundamental period, a condition that changes during disturbances.

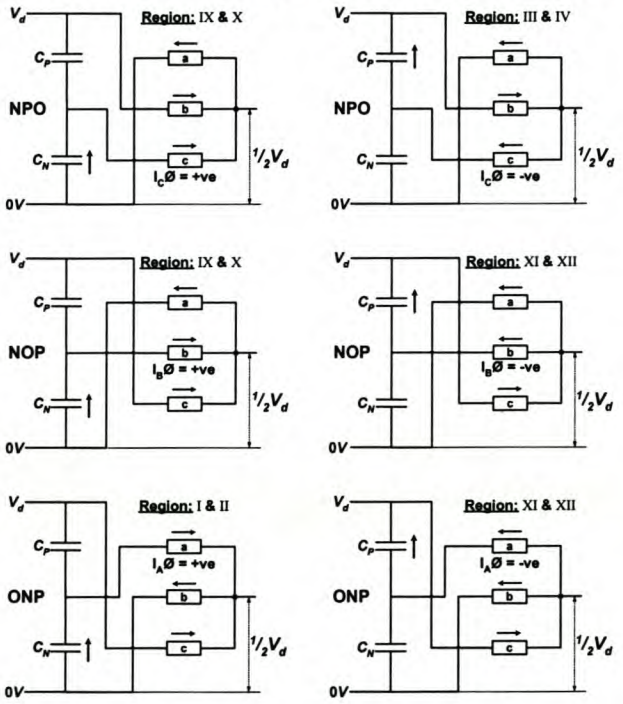


Figure 5-27: Medium Voltage Switching States of the 3-Level Converter, States NPO, NOP & ONP

The last observation for these switching states, in both Figure 5-26 and Figure 5-27, is that when there is no current flowing in the phase-arm selected in a '0' state, the star point voltage is $\frac{1}{2}V_d$. This indicates that the largest voltage over a load, using this switching state, is typically $\frac{1}{2}V_d$. During the aforementioned states the freewheeling currents flowing in the capacitors cause the neutral point voltage to vary. This has an undesired impact on the amplitudes of the three-phase voltages being modulated when switching other states. Transforming these switching states into the α-β plane, i.e. using the three-phase values in the regions specified by Figure 5-26 and Figure 5-27 in Figure 5-24, results in vectors that have a smaller numeri-

cal value than the large switching vectors, thus the name medium voltage vectors. It is important to note that the converter switching states are still under discussion. The voltage vectors mentioned refer to switching states defined as vectors in the α-β plane.

Finally the last of the states identified in Table 5 is that of the small voltage vectors. These are once again divided into the upper small voltage switching states, Figure 5-28, and the lower small voltage switching states, Figure 5-29.

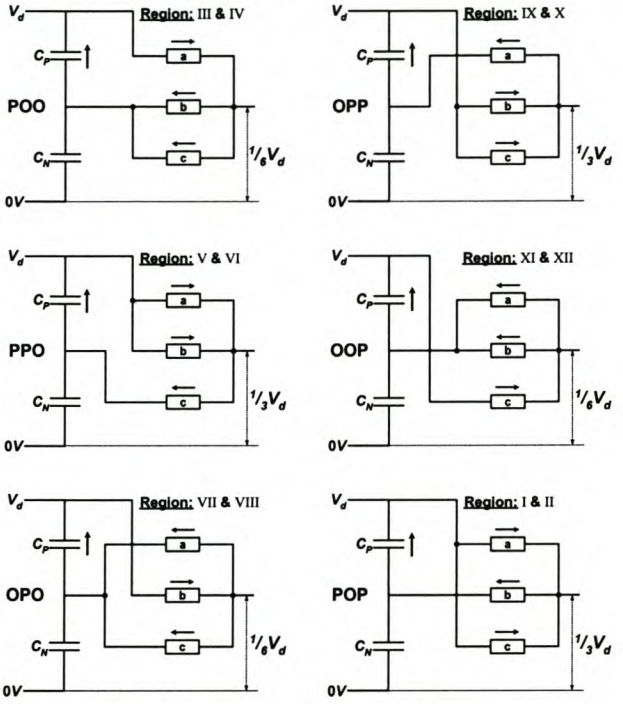


Figure 5-28: Upper Small Voltage Switching States of the 3-Level Converter

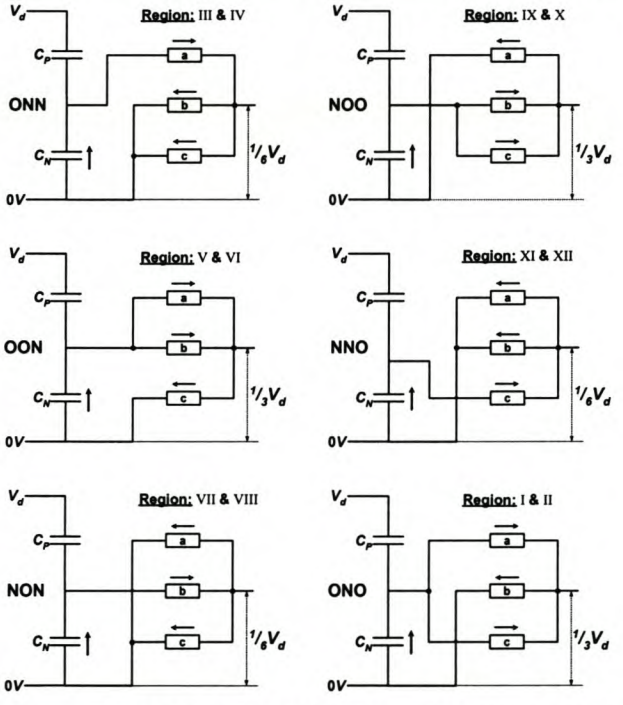


Figure 5-29: Lower Small Voltage Switching States of the 3-Level Converter

The naming of the upper small voltage vectors is indicative of their connection to the upper

capacitor cell C_P, seen in Figure 5-28. By switching the converter into state OPP, the load is only subjected to half the full DC bus value. The subsequent voltages achievable over any of the phase loads are $^1/_3 V_d$. This is exactly half of the magnitude achievable when selecting the large voltage vectors in Figure 5-25.

In comparison, the two small voltage switching states, the upper and the lower, share a number of features. The first commonality is that for the state OPP and the state NOO. In these states the currents flow through the loads in the same direction. This suggests that the switching states occur in the same regions, verified in Figure 5-24. The largest variation is that of the current paths. Each of these two states affects different limbs of the DC bus capacitors. State OPP causes current to flow through C_P, while state NOO causes the current to flow through C_N. Similar to the medium voltage vectors, each of these states has the ability to destabilise the centre point of the converter. Unlike the medium voltage vectors, the small vectors occur in the same regions.

Thus during the same region it is possible to draw energy from both C_P and C_N. This implies that by toggling between the two small voltage switching states, it is possible to cancel out the effect on the converter's centre point, a task not possible with the medium voltage switching states.

Converting these 27 switching states into the two-phase plane is achieved using the α-β transform (5.1) [44][45][46][47]. From the discussions of the various switching states, it is observed that each of the states has an operating range. These ranges are symmetrical around a certain axis in the three-phase plane. By substituting the values at these axes into the transform, the switching vectors for these states are obtained, as seen in Figure 5-30.

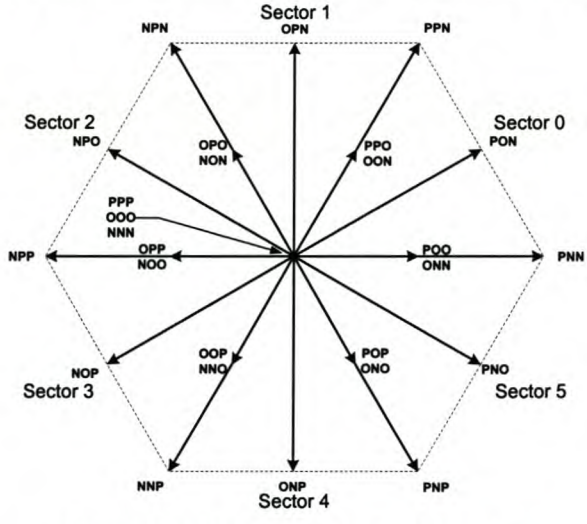


Figure 5-30: 3-Level SVM State Vectors

In Figure 5-30 the location of the zero, small, medium and large voltage vectors can clearly be seen. As was the case for the 2-level SVM, each 60° segment is named, from Sector 0 to Sector 5. A closer inspection of Sector 0 is seen in Figure 5-31, where each sector is divided into four regions.

5.3.1.1 Regional Determination of V_{ref}

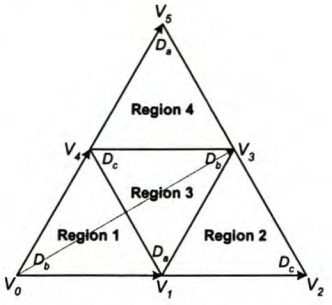


Figure 5-31: Regions and State Vectors within Sector 0 for 3-Level SVM

In each region, the three closest state vectors to that region are used to generate the required reference vector, V_{ref}, supplied by the control system. So as the reference vector steps through each region, the choice of the switching vectors used changes. The reference vector is once again specified in terms of the modulation index, m_a, and the angle, θ, the typical scenario seen in Figure 5-32.

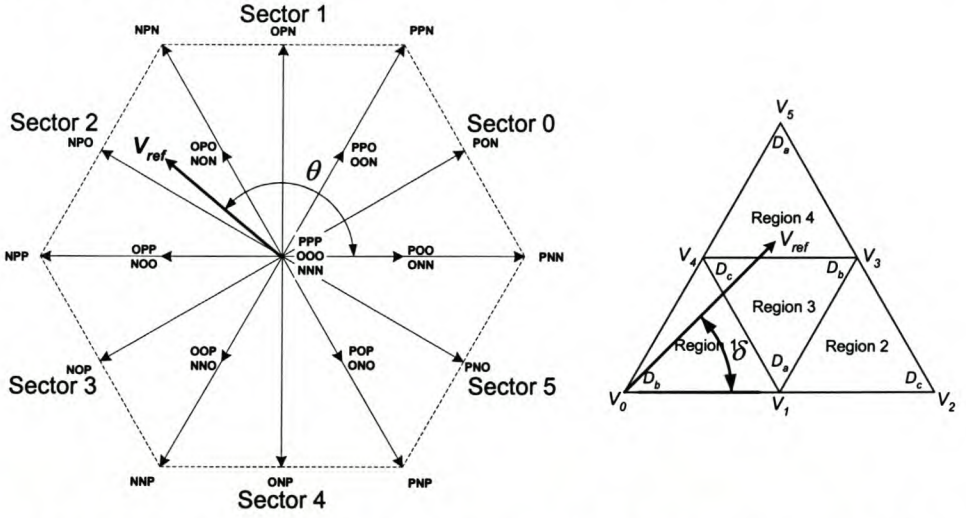


Figure 5-32: Referring the Reference Vector back to Sector 0 for 3-Level SVM

As was the case for the 2-level SVM, the circular symmetry of the vectors allow the referral of V_{ref} and θ back to Sector 0, in order to determine the relevant duty cycles. Once again V_{ref}'s angle, θ, is modified to become the angle δ. The next step is to calculate in which region of Sector 0 the vector V_{ref} resides. Although various methods are used [76][77][78], the alternative chosen was that using equations that determined the region from the modulation index, m_a, and the modified angle, δ.

Figure 5-33 is used to determine the relevant equations for region determination. The large voltage vectors are chosen to have a unity length, i.e. the size of the DC bus value. Using p.u. values, the maximum obtainable value for the medium voltage vector is $\sqrt{3}/2$, also shown in the 2-level SVM explanations. The maximum small voltage vector length now becomes ½. Using these identities, it is also possible to determine the maximum output voltage in the three-phase plane.

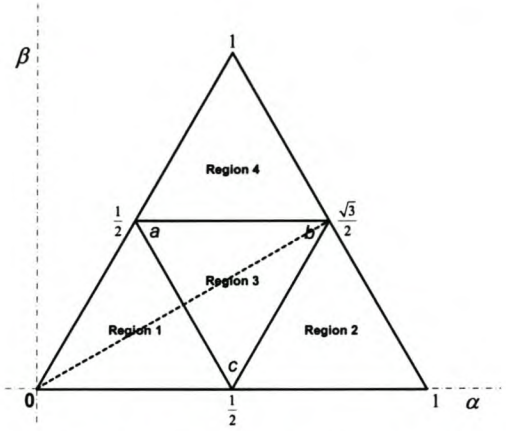


Figure 5-33: Vector Lengths for Sector 0, used throughout 3-Level SVM Theory

In preventing the converter from over modulation, i.e. trying to modulate a voltage for longer than the allotted switching period [68], the maximum vector length is $\sqrt{3}/2$ p.u. Since p.u. values move in and out of the Clarke Transform unaffected, the maximum AC voltage that can be modulated using SVM is $\sqrt{3}/2 V_d$.

With the size and angle of V_{ref} changing according to the controller's requirements, it is necessary to mathematically determine the region boundaries. Determining the boundary for Region 1 is achieved by defining the line *a-c* in Figure 5-33 with respect to m_a and δ. The function for line *a-c* defined on the α and β plane is:

$$\beta = -\sqrt{3} \cdot \alpha + \frac{\sqrt{3}}{2}$$

Converting this into polar form yields the following:

$$r \angle \delta = \alpha + j \cdot \beta$$

$$\therefore \beta = r \cdot \sin\delta \quad \text{AND} \quad \alpha = \cos\delta$$

$$r \cdot \sin\delta = -\sqrt{3} \cdot (r \cdot \cos\delta) + \frac{\sqrt{3}}{2}$$

$$r \cdot (\sin\delta + \sqrt{3} \cdot \cos\delta) = \frac{\sqrt{3}}{2}$$

Using the identities:

$$\cos\frac{\pi}{3} = \frac{1}{2} \quad AND \quad \sin\frac{\pi}{3} = \frac{\sqrt{3}}{2}$$

The following is achieved:

$$2r \cdot \left(\frac{1}{2} \cdot \sin\delta + \frac{\sqrt{3}}{2} \cdot \cos\delta \right) = \frac{\sqrt{3}}{2}$$

$$2r \cdot \left(\cos\frac{\pi}{3} \cdot \sin\delta + \sin\frac{\pi}{3} \cdot \cos\delta \right) = \frac{\sqrt{3}}{2}$$

$$r \cdot \sin\left(\delta + \frac{\pi}{3} \right) = \frac{\sqrt{3}}{4} \tag{5.15}$$

From the 2-level SVM theory the following was proved:

$$V_{ref} = m_a \cdot \frac{\sqrt{3}}{2} \cdot V_d \tag{5.16}$$

V_d is set as the unity value as seen in Figure 5-33.

$$\therefore V_{ref} = \left(\frac{\sqrt{3}}{2}\cdot m_a\right)\cdot e^{j\delta} = r\cdot e^{j\delta} = r\angle\delta$$
$$\therefore r = \frac{\sqrt{3}}{2}\cdot m_a \tag{5.17}$$

Substituting (5.17) into (5.15) yields:

$$2\cdot m_a\cdot\sin\left(\frac{\pi}{3}+\delta\right)=1$$

Since the reference has to be smaller than the boundary line *a-c* for it to fall into Region 1, the following formula is derived:

$$2\cdot m_a\cdot\sin\left(\frac{\pi}{3}+\delta\right)<1$$

In Region 2 of Figure 5-33, using the boundary line *b-c*, the following boundary equation for the region was obtained:

$$2\cdot m_a\cdot\sin\left(\frac{\pi}{3}-\delta\right)>1 \quad \textit{for the boundary line function } \beta=\sqrt{3}\cdot\alpha-\frac{\sqrt{3}}{2}$$

While the boundary equation for Region 4 was derived as:

$$2\cdot m_a\cdot\sin\delta>1 \quad \textit{for the boundary line function } \beta=\frac{\sqrt{3}}{4}$$

For all other conditions, where the reference vector does not comply with the derived equations, the vector is assumed to be in Region 3.

The procedure followed is thus first locating the sector in which V_{ref} appears, referring it back to Sector 0, then subjecting V_{ref}, using its m_a and angle δ, to the equations below in order to determine its region.

Reference is in Region 1 if: $2\cdot m_a\cdot\sin\left(\frac{\pi}{3}+\delta\right)<1$ (5.18)

Reference is in Region 2 if: $2\cdot m_a\cdot\sin\left(\frac{\pi}{3}-\delta\right)>1$ (5.19)

Reference is in Region 4 if: $2\cdot m_a\cdot\sin\delta>1$ (5.20)

Reference is in Region 3 if: None of the above equations are satisfied (5.21)

With the regional location determined, duty cycles for the switching states, within the specified region, need to be calculated.

5.3.1.2 Duty Cycle Calculations for 3-Level SVM

Once again it is necessary to consider the different regions within Sector 0, seen in Figure 5-34. The placing of the vectors in Figure 5-34 are an important observation, since they are used in the formulation of numerous duty cycle equations in the section that follows. Inspection of each region shows the presence of the three duty period components that make up the full switching period, displayed in equation (5.22). This condition is used in the calculations of all relevant duty cycles, in all four regions.

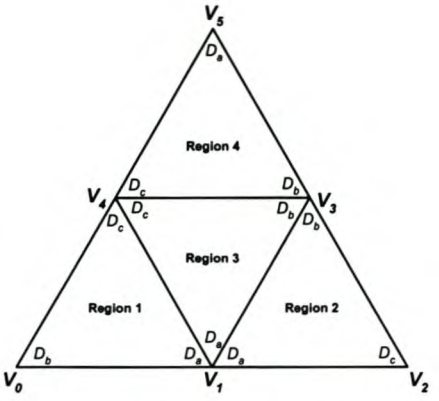


Figure 5-34: Vector and Duty Cycle Placement, used throughout 3-Level SVM Theory

$$D_a + D_b + D_c = 1 \tag{5.22}$$

Also of relevance is the definition of the reference vector, its polar format defined as:

$$r\angle\delta = r\cdot(\cos\delta + j\sin\delta) \tag{5.23}$$

Furthermore it was seen in the normal 2-level SVM theory that the reference vector, V_{ref}, can be represented as a p.u. value and can be represented as the following:

$$V_{ref} = V\cdot e^{j\delta} \quad with \quad V = \frac{\sqrt{3}}{2}\cdot m_a \tag{5.24}$$

For all the formulas derived for the four regions, the following standard trigonometric identities are extensively used.

$$\begin{aligned} &\sin\frac{\pi}{3} = \frac{\sqrt{3}}{2} \quad AND \quad \sin\frac{\pi}{6} = \frac{1}{2} \\ &\cos\frac{\pi}{3} = \frac{1}{2} \quad AND \quad \cos\frac{\pi}{6} = \frac{\sqrt{3}}{2} \end{aligned} \tag{5.25}$$

Using the above identities and formulae, the duty cycles for each region can be calculated.

5.3.1.2.1 Derivation of the Duty Cycle Formulae for Region 1

Each region within Figure 5-34 has a unique equation used to replicate the given V_{ref} supplied from the control system. These equations are derived from Figure 5-34 and identity (5.22), and can be represented as follows:

$$V_0\cdot D_b + V_1\cdot D_a + V_4\cdot D_c = V_{ref} \tag{5.26}$$

In Region 1 the vector lengths of equation (5.26) have the following values, obtained from the per unit values seen in Figure 5-33.

$$V_0 = 0 \quad AND \quad V_1 = \frac{1}{2} \quad AND \quad V_4 = \frac{1}{2}\cdot e^{j\frac{\pi}{3}}$$

Using (5.23) and (5.26) the following solution is obtained:

$$\frac{1}{2}\cdot D_a + \frac{1}{2}\left(\cos\frac{\pi}{3} + j\sin\frac{\pi}{3}\right)\cdot D_c = V\cdot(\cos\delta + j\sin\delta)$$

Separating these values into their real and imaginary components and applying the identities in (5.25) to these real and imaginary values yields the following:

$$\text{Re}:\ \frac{1}{2}\cdot D_a + \frac{1}{4} = V\cos\delta \quad AND \quad \text{Im}:\ \frac{\sqrt{3}}{4}\cdot D_c = V\sin\delta$$

A matrix can then be constructed using the real and imaginary parts of the above solution and (5.26). The matrix is as follows:

$$\begin{bmatrix} 1 & 1 & 1 \\ \frac{1}{2} & 0 & \frac{1}{4} \\ 0 & 0 & \frac{\sqrt{3}}{4} \end{bmatrix} \cdot \begin{bmatrix} D_a \\ D_b \\ D_c \end{bmatrix} = \begin{bmatrix} 1 \\ V\cos\delta \\ V\sin\delta \end{bmatrix} \tag{5.27}$$

Solving the equation with the least unknowns, and substituting identity (5.24) into that equation, a formula for the duty cycle D_c is obtained.

$$D_c = 2m_a \cdot \sin\delta \tag{5.28}$$

Equation (5.28) is then used to solve D_a, and is substituted into the second row of the matrix in (5.27). It yields the following:

$$\frac{1}{2}D_a = V \cdot \left(\cos\delta - \frac{1}{\sqrt{3}}\sin\delta\right)$$

Using the standard trigonometric identities in (5.25) and the Sine rule, the equation can be simplified as follows:

$$D_a = V \cdot \left(2\cos\delta - \frac{2}{\sqrt{3}}\sin\delta\right)$$

$$= \frac{4}{\sqrt{3}}V \cdot \left(\frac{\sqrt{3}}{2}\cos\delta - \frac{1}{2}\sin\delta\right)$$

$$= \frac{4}{\sqrt{3}}V \cdot \sin\left(\frac{\pi}{3} - \delta\right)$$

Once again applying (5.24) the following is obtained:

$$D_a = 2 \cdot m_a \cdot \sin\left(\frac{\pi}{3} - \delta\right) \tag{5.29}$$

Applying the solutions from (5.28) and (5.29) into the matrix (5.27) gives rise to the solution below. D_b is simplified using the trigonometric identities from (5.25) and the Sine rule.

$$D_b = 1 - \frac{4}{\sqrt{3}}V \cdot \left(\frac{\sqrt{3}}{2}\cos\delta - \frac{1}{2}\sin\delta\right) - \frac{4}{\sqrt{3}}V\sin\delta$$

$$\therefore D_b = 1 - \frac{4}{\sqrt{3}}V \cdot \sin\left(\frac{\pi}{3} + \delta\right)$$

Finally using (5.24) the following equation is derived:

$$D_b = 1 - 2 \cdot m_a \cdot \sin\left(\frac{\pi}{3} + \delta\right)$$

In conclusion, the duty cycle formulas for Region 1, represented in terms of m_a and δ, is expressed as follows:

$$D_a = 2 \cdot m_a \cdot \sin\left(\frac{\pi}{3} - \delta\right) \tag{5.30}$$

$$D_b = 1 - 2 \cdot m_a \cdot \sin\left(\frac{\pi}{3} + \delta\right) \tag{5.31}$$

$$D_c = 2 \cdot m_a \cdot \sin\delta \tag{5.32}$$

Similarly, for the other three regions, Regions 2 to 4, equations for their duty cycles are formulated, using the same process as used for Region 1. The process of solving these duty cycles is discussed in detail in Appendix B. Determining of the duty cycles for Regions 2 to 4 is more complex than that of Region 1, and Gaussian elimination is used to simplify the matrices. The duty cycle equations are summarised as the following:

5.3.1.2.2 Duty Cycle Formulae for Region 2

$$V_1 \cdot D_a + V_3 \cdot D_b + V_2 \cdot D_c = V_{ref} \tag{5.33}$$

Using (5.33) the following equations can be determined:

$$D_a = 2 - 2 \cdot m_a \cdot \sin\left(\frac{\pi}{3} + \delta\right) \tag{5.34}$$

$$D_b = 2 \cdot m_a \cdot \sin\delta \tag{5.35}$$

$$D_c = 2 \cdot m_a \cdot \sin\left(\frac{\pi}{3} - \delta\right) - 1 \tag{5.36}$$

5.3.1.2.3 Duty Cycle Formulae for Region 3

$$V_1 \cdot D_a + V_3 \cdot D_b + V_4 \cdot D_c = V_{ref} \tag{5.37}$$

Using (5.37) the following equations can be determined:

$$D_a = 1 - 2 \cdot m_a \cdot \sin\delta \tag{5.38}$$

$$D_b = 2 \cdot m_a \cdot \sin\left(\delta + \frac{\pi}{3}\right) - 1 \tag{5.39}$$

$$D_c = 2 \cdot m_a \cdot \sin\left(\delta - \frac{\pi}{3}\right) + 1 \tag{5.40}$$

5.3.1.2.4 Duty Cycle Formulae for Region 4

$$V_5 \cdot D_a + V_3 \cdot D_b + V_4 \cdot D_c = V_{ref} \tag{5.41}$$

Using (5.41) the following equations can be determined:

$$D_a = 2 \cdot m_a \cdot \sin\delta - 1 \tag{5.42}$$

$$D_b = 2 \cdot m_a \cdot \sin\left(\frac{\pi}{3} - \delta\right) \tag{5.43}$$

$$D_c = 2 - 2 \cdot m_a \cdot \sin\left(\frac{\pi}{3} + \delta\right) \tag{5.44}$$

Using these formulae, in conjunction with the equation for sector and region determination, 3-level SVM can finally be implemented on the NPCC converter topology, seen in Figure 5-22. Using Figure 5-35 as an example, the process of modulating the reference vector in Sector 2 can be summarised as follows. The first step is the determination of the angle θ. Thereafter θ is rotated back to Sector 0 and δ is calculated. The region in which the reference vector is located, in Figure 5-35, is found to be Region 4, and this is verified by equation (5.20). The duty cycles are then calculated using equations (5.42) to (5.44).

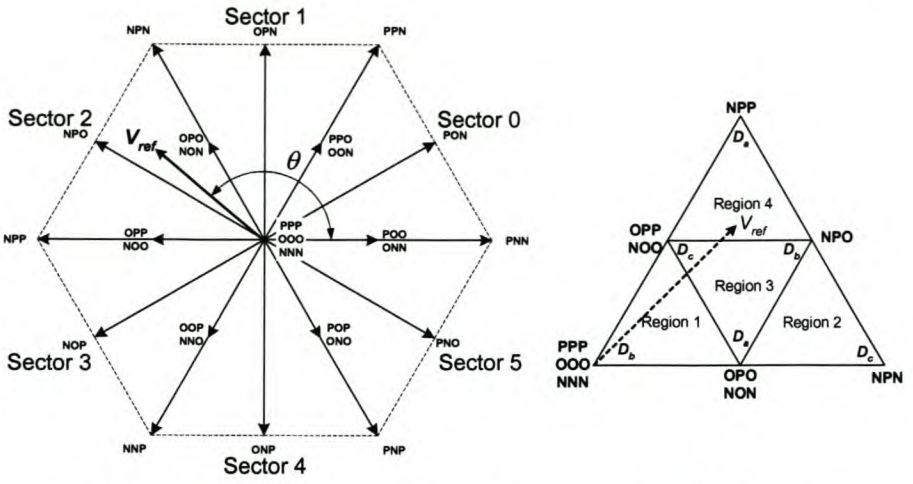


Figure 5-35: 3-level SVM - Sector 2 - Region 4 - Switching States

Using the switch selection of Sector 2 - Region 4, also illustrated in Figure 5-35, the duty cycles can be implemented. For this example the switching sequence would be as follows: OPP→NPP→NPO. Equation (5.42) is used to calculate the conduction time for switch state OPP, (5.43) for state NPO and (5.44) for NPP. The sequence chosen within a region is that of the smallest switching vector first and thereafter the large switching vector and finally the medium vector. The sequence is chosen to ensure that the smallest number of state changes occur during switching, thereby reducing the switching harmonics. Previous investigations into the natural balancing of the NPCC verified that this switching sequence produced the least amount of switching harmonics and most stable operation [75]. Furthermore, the small switching vectors are also alternated, ensuring the smallest impact on the DC bus capacitors during the use of the small voltage vector switching states. Typically the switching state within Region 4 would be NOO→NPO→NPP.

The associated duty cycle modulation functions of the 3-level SVM switching technique are seen in Figure 5-36. The symmetry of the duty cycle functions is clearly seen.

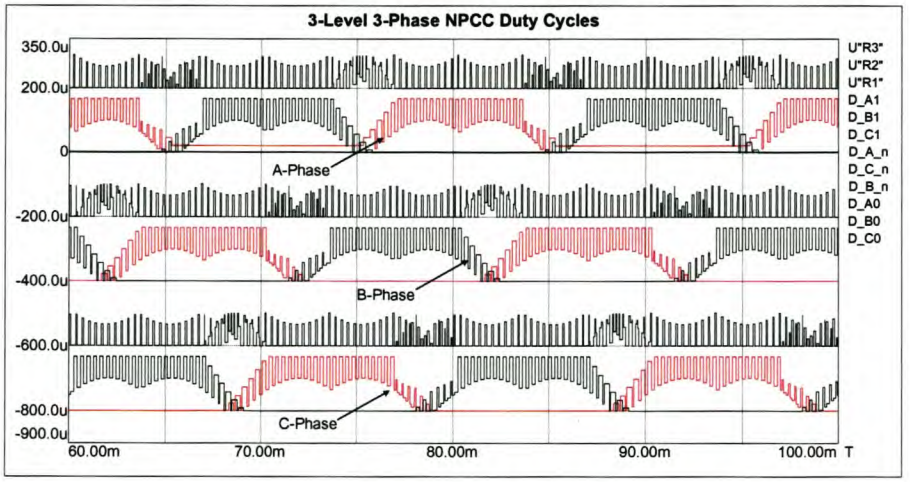


Figure 5-36: Typical 3-Level SVM Duty Cycle Modulation Functions

A closer inspection is seen in Figure 5-37 where the output to the B-phase is shown exclusively. The three outputs shown are the outputs for each individual state, namely the 'P'

state, 'N' state and the '0' state.

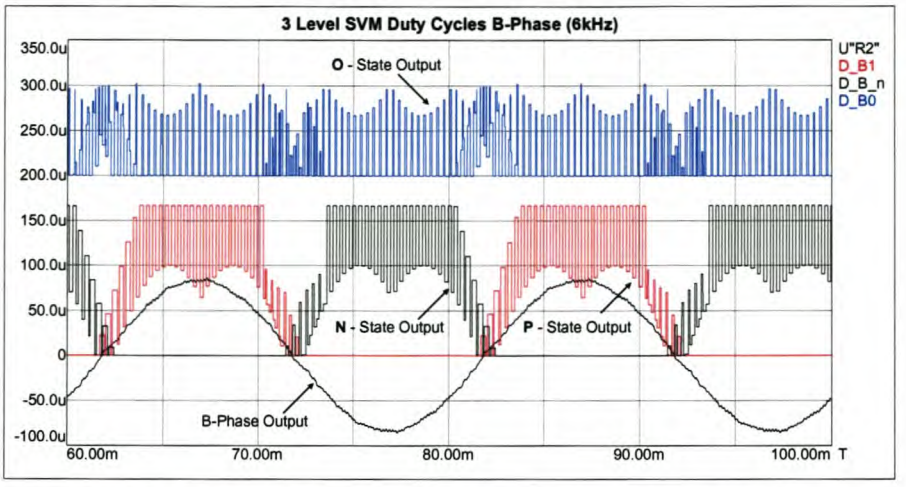


Figure 5-37: 3-Level SVM Duty Cycle Modulation Function – B-Phase

The '0' state is also offset by 200μs. Closer inspection of the functions shows what appears to be a maximum 'ON' time of 166μs, clearly observed in the 'P' and 'N' states. This implies that the B-phase switch is kept in this position for a full switching period. During the next switching period, the switch state stays constant for only a portion of the switching period and then changes state. This is attributed to the switching sequence chosen, where switches are required to maintain their status for longer than the 166μs switching period. This condition can also be viewed in the simulation model state machines found in Appendix A. In Figure 5-37 the typical modulated B-phase waveform is also superimposed on the figure, to show its relevant phase positioning. The 'P' state modulation period coincides with the positive half of the waveform, while the 'N' state modulation coincides with the negative half of the waveform.

5.3.2 Balancing concerns of the NPCC

Unbalancing implies that the two DC bus capacitors fail to share the DC bus voltage evenly. This results in unstable operation, as the waveforms cannot be modulated evenly. For the NPCC, unbalancing is a result of current flowing back up the neutral path, through either capacitor C_P or C_N [55], whist using medium and small voltage switching vectors. Even with the average neutral point current being zero and with stable DC bus voltages, equal sharing of the voltages by the capacitors is not guaranteed. System transients, large load steps, component imperfection and operation at high modulation indices influence the balancing. Alternatively, during steady state operation, the capacitor voltages are influenced by the output filter and load, as well as switching functions derived from the converter switch states [56].

It has also been proven that switching the medium voltage vector results in unbalance, since positive and negative small voltage vectors can be switched alternately, cancelling out their effect on the capacitor. The medium voltage vector has no negative state.

A frequency component, occurring at half the converter switching frequency, is also associated with the NPCC [56]. Its presence is attributed to the switching vector selection used in the 3-level SVM, an important consideration for reducing the unbalance. The frequency component's origin is best understood by noting that a switching frequency variation occurs when using 3-level SVM. This is because of the sequence used when switching between positive small vectors and negative small vectors. For example, when switching at 6 kHz in Sector 1, Region 4, and using a positive small voltage vector, the following sequence is used: PPO→PPN→PON. This is done so that only one IGBT is switched during each step, reducing the switching harmonics. Toggling to the negative small voltage vector results in the next sequence chosen to be OON→PON→PPN. The net effect on the A and C-phase IGBTs is that they only change state every second switching period. Therefore these switches operate at a switching frequency of 3 kHz while the B-phase IGBT operates at 6 kHz during this region. When the reference moves to the next region, the sequence and switch operating frequencies change. During this sequence, the cancelling effect of the small switching vectors is observed, while the impact of the medium switching vector, having no negative state, is also apparent.

Although the NPCC possesses natural balancing mechanisms, caused by system losses, the balancing can be improved by making use of a balance booster. The balance booster, connected over the load, consists of a series capacitor-inductor connection that acts as a band pass filter, providing a low impedance path for the harmonic occurring at half the switching frequency. The balance booster was, however, not used in the comparative studies of this thesis, since it is not required for operation of the SSC.

5.3.3 3-level SVM Implementation on the NPC Converter

Applying the 3-Level SVM to the converter model to evaluate its performance is the next required step. The simulation model, details of which are to be found in Appendix A, was implemented on a 3-level NPCC topology like that seen in Figure 5-38.

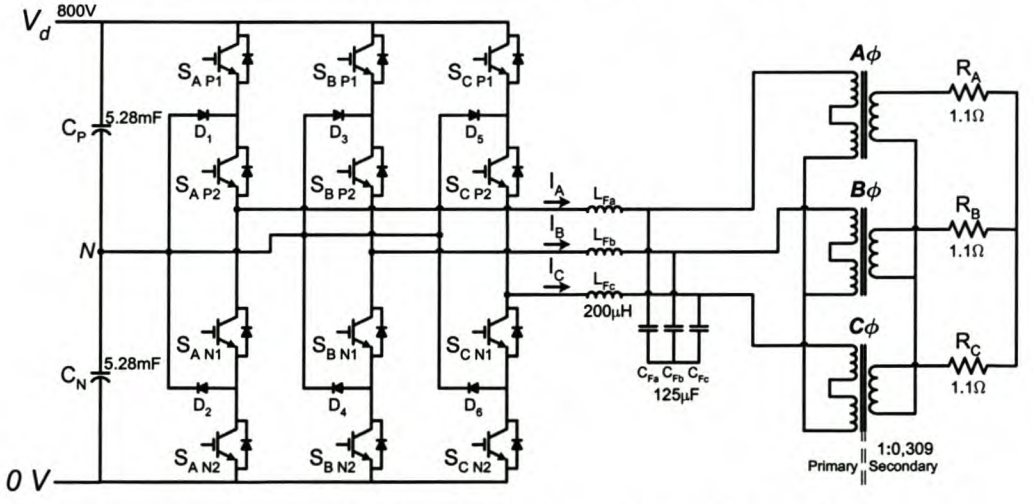


Figure 5-38: The 3-Level Neutral Point Clamped Converter

Re-examination of the topology shows that the converter uses 12 switches, 4 per phase-arm, to obtain the three output voltage levels per phase. The only unnecessary portion of the model is that of the transformer, but to minimise the comparative differences between the SSC and NPCC the transformer is added.

Using the gating pulses, created using the 3-level SVM theory investigated in the previous section, the converter operation was simulated using SIMPLORER® and the simulation parameters seen in Table 6. The parameters are identical, with the exception that the filter inductance is double that of the SSC simulation model. The transformer ratio is modified to compensate for the increased input voltage. Terminal connections on the primary side are changed from a 3-winding transformer, used in the SSC, to a 2-winding transformer, seen in Figure 5-38.

The output voltages are identical to those of the SSC. This is necessary since the NPCC output is twice the size of the individual converter units of the SSC.

Table 6: SSC Simulation Parameters Using Normal SVM

Components	Values
DC Bus	840 V
Switches	Ideal
Filter Inductors	200 µH
Filter Capacitors	125 µF
Transformer Ratios	1: 0.309
Load Resistance	1.1 Ω
Switching Parameters	
Modulation Index	0.8
Switching Frequency	6 kHz

Using a reference vector with a m_a of 0.8 p.u. and rotating it through 360° using 120 steps, simulates the 6 kHz switching frequency modulating the 50 Hz fundamental. Applying the switch selection process previously discussed results in the simulation output waveforms seen in Figure 5-39.

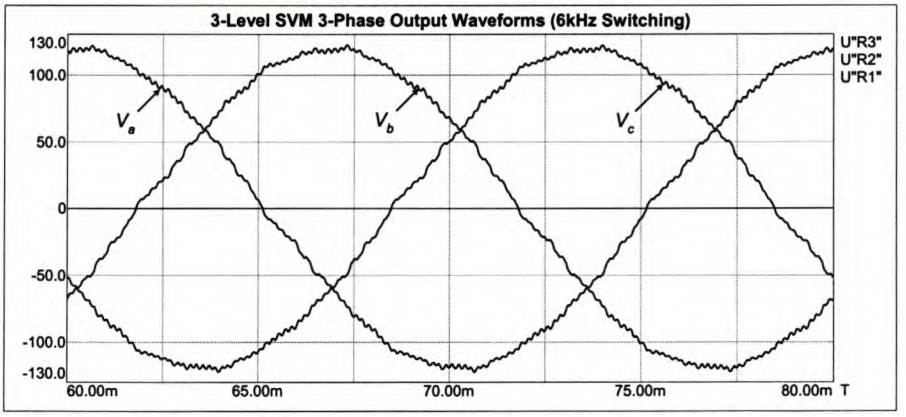


Figure 5-39: 3-Level SVM 3-Phase Output Voltage Waveforms

The waveforms of the simulation yield good quality three-phase voltage waveforms with limited waveform distortion. The distortion is attributed to the switching sequences encountered at the sector boundaries. During these changeover states, more than one switch state usually has to change state. This results in increased switching harmonics and can lead to instability, if the wrong sequence is chosen.

5.4 Benefit of P.U. Reference Values

The benefit of using a reference value, V_{ref}, as a p.u. value for all the control strategies becomes apparent when considering the benefit of using SVM. SVM has the unique characteristic in that the values in the α-β plane are totally de-coupled. This permits the individual control of either of the quantities. A required reference value can thus be chosen in the three-phase plane and be transformed into the α-β plane, and two separate de-coupled α-β values are generated. Furthermore, the resultant waveforms generated, the counter Emf, using the SVM technique, can be measured and the error between the required α-β values and the measured α-β values can be compensated for.

A wide variety of compensation strategies now present themselves as possible solutions. One alternative is that of using a predictive current controller within the α-β plane. The technique was originally designed for operation of de-coupled and bipolar operating converters [72]. Looking at Figure 5-40, it is possible to regulate the individual α-β current values by using the predictive current control technique.

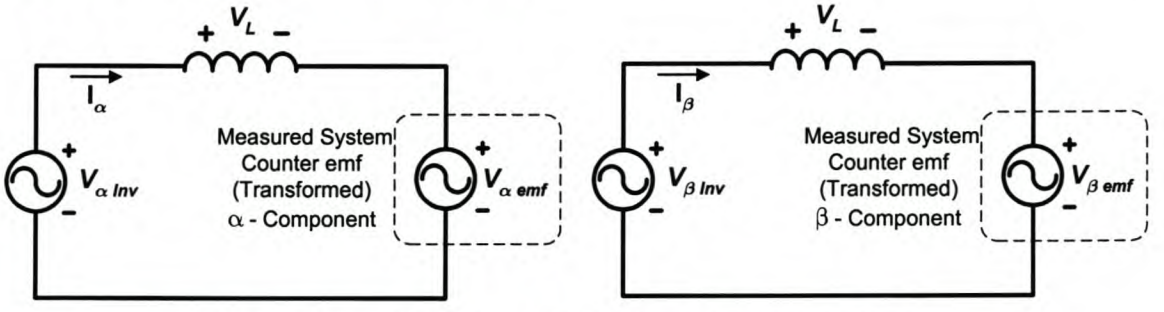


Figure 5-40: Individual Control of Currents Within the α-β Plane

Using the models in Figure 5-40 and the equations in (5.45) it is possible to create a current controller. This is obtained by the measurement of the error in the current magnitude ($i_{\alpha\ Reference}$ - $i_{\alpha\ Measured}$), which in turn provides information as to the size of the required di_α.

$$V_{\alpha\ inv} - L\frac{di_\alpha}{dt} - V_{\alpha\ emf} = 0 \qquad AND \qquad V_{\beta\ Inv} - L\frac{di_\beta}{dt} - V_{\beta\ emf} = 0 \tag{5.45}$$

Alternatively, the technique proposed by Akagi [43] offers the ability to control the instantaneous reactive power, a characteristic desired when performing shunt compensation. The technique uses the set of equations below to determine the instantaneous active and reactive α and β currents.

$$\alpha - axis\ inst.\ active\ current : i_{\alpha p} = \frac{e_\alpha}{{e_\alpha}^2 + {e\beta}^2} \cdot p$$

$$\alpha - axis\ inst.\ reactive\ current : i_{\alpha q} = \frac{-e_\beta}{{e_\alpha}^2 + {e\beta}^2} \cdot q$$

$$\beta - axis\ inst.\ active\ current : i_{\beta p} = \frac{e_\beta}{{e_\alpha}^2 + {e\beta}^2} \cdot p$$

$$\beta - axis\ inst.\ reactive\ current: i_{\beta q} = \frac{e_\alpha}{{e_\alpha}^2 + {e\beta}^2} \cdot q$$

Where p and q are the instantaneous active and reactive power elements of the measured output and e the instantaneous voltage. Regulation of the instantaneous reactive currents permits reactive power to be compensated for. This is typically performed during shunt compensation.

Using these, two of a number of possibilities, it is possible to generate reference values in p.u. form and thus apply them to both converter topologies. Both topologies can thus use the same control strategy, which supplies the reference value to the necessary switching technique, 2-level or 3-level SVM. Using current regulators, both converters can be operated in the inverting and rectifying modes. It is the converters' capability to perform either of these functions on demand that makes them suitable for power quality mitigation and modification functions, like those discussed in Chapter3.

5.5 Chapter Summary

This chapter discussed the SSC and NPCC topology considerations when implementing Space Vector Modulation. A broader understanding of the various switching states, and the associated effects, for both topologies is obtained. Formulae for both 2 and 3-level SVM switching schemes have derived and evaluated, using simulation models the duty cycles have been calculated with the aforementioned formulae. Discussions on DC bus unbalance concerns for both topologies were discussed, with the NPCC proving to be the most affected topology. The benefit of using a reference vector, that is specified in terms of the modulation index, m_a, and an angle, θ, for both topologies and switching schemes, is shown. The next step is to obtain practical converter measurements in order to compare them with the current simulation models.

Chapter 6 Practical Topology Comparisons

6.1 Introduction

This chapter investigates the practical operation of the SSC and the NPCC. A brief overview of the practical converter, its construction and the control devices used is performed. Thereafter the basic operation is investigated, essentially to provide information of the switching operation, behaviour and topological characteristics. More detailed analysis is performed on the various topological modulation capabilities, identifying beneficial characteristics, and quality of the waveforms, while using open-loop control and switching into a resistive load. Open-loop control is opted for, since closed-loop control will suppress any phenomena associated with either of the topologies and their switching techniques. Finally the impact of each of the topologies on various essential components within the converter is analysed, in order to determine trends and basic design guidelines.

6.2 Practical Converter Construction

Accurate comparisons require that both topologies are not only subjected to the identical loading conditions, but should also be constructed in a similar manner. This ensures that parasitic component effects and losses occurring in the converter are experienced by both topologies. This resulted in one re-configurable converter structure being built. To further limit expenses, components from previous projects were used in the construction of the converter.

Table 7: Re-Configurable Converter Components

Component	Ratings In System	Description
12 IGBTs ($S_{X\,P1}$-$S_{X\,N2}$)	1200 V / 400 A	POWEREX - PM400HSA120
6 Freewheeling Diodes (D_1-D_6)	1200 V / 300 A	SEMIKRON - SKMD150F
40 DC Bus Capacitors (C_P)	5.28 mF	L.C.R. – 3300 µF, 450 V Each
40 DC Bus Capacitors (C_N)	5.28 mF	L.C.R. – 3300 µF, 450 V Each
2 Filter Inductors (SSC)	100 µH / 400 A	3ϕ - Laminated Steel Core
1 Filter Inductor (NPCC)	200 µH / 400 A	3ϕ - Laminated Steel Core
2×30 3ϕ Filter Capacitors (C_{FX})	125 µF	AFCAP – C.V.T. 440 V, 5 µF Each
6 Isolation Transformers	140:140:140:260 V / 24.2 kVA	1-Phase 4-Winding - Laminated Steel
Transformer Ratios (SSC)	1: 1: 0.619 (3-Winding)	Paralleled Input & Output
Transformer Ratios (NPCC)	1: 0.309 (2-Winding)	Series Input, Parallel Output
Isolated Power Supplies	3 kV Isolation / 20 kHz	Provides Supply for Gate Drives
Isolated Gate Drives	Optical Interface	Gate Receive / Error Feedback
Snubbers	Clamps at 730 V	Diode / Capacitor / Resistor / Tranzorb
PEC31 Controller	50 MHz DSP & FPGA	In-House Developed Controller
PEC Optical Board	Fibre Optic	Optical Transmit & Receive Board

A list of the various components on the re-configurable converter and a brief description is

tabulated in Table 7. Originally designed to operate at approximately 300 A, the unit was de-rated to accommodate the available isolation transformers, whose voltage and power ratings would have been exceeded. Re-configuration, being the primary objective, results in large parasitic components within the converter. Although undesired, the impact is tolerable in the comparison of the topologies. This ensures that comparative measurements are not affected by more efficient converter designs.

The inductor values chosen also warrant further discussion. This, however, requires that the isolation transformers be discussed first. It should also be noted that the transformer primary refers to the connections on the converter side and the secondary refers to the load side. Each transformer unit consists of 3 primary 140 V windings and 1 secondary 260 V winding. In order to operate at an 800 V DC bus, the primary windings in the SSC are required to exceed 400 V at least. This is achieved by connecting the three 140 V primary windings of each individual transformer in series.

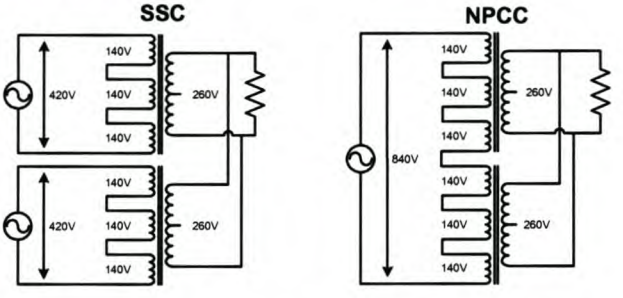


Figure 6-1: SSC and NPCC Per Phase Transformer Connections

Two isolation transformers, connected like those seen for the SSC in Figure 6-1, are used per phase when configured as an SSC. The secondary is paralleled to the load, yielding the 1:1:0.619 turns ratio. For the NPCC, each primary winding is required to be 800 V. The primaries of the two isolation transformers are externally connected like those seen in Figure 6-1 for the NPCC. This results in a 1:0.309 turns ratio. Looking back into the transformer from the secondary, the inductor values are required to have the same impedance reflected on the secondary. The combination of the parallel inductors and the transformer winding ratio results in the SSC requiring the two 100 μH inductors, as opposed to the single 200 μH inductor for the NPCC.

The filter capacitors were originally selected to operate on the transformer's primary side. However, more information on the switching techniques is obtained while they are connected on the secondary side of the transformer. Secondary connection and in conjunction with the reflected primary filter inductance, they form a low-pass filter with a cut-off frequency of 3.258 kHz. This frequency was higher than planned for, but this value was kept since the switching frequency of both the SSC and the NPCC was selected as 6 kHz and identical operating conditions were the key.

6.2.1 Re-Configurable Converter Structure

(A) SSC (B) NPCC

Figure 6-2: Practical Converter Configurations

The constructed converter, connected in both SSC and NPCC configurations, is seen in Figure 6-2. The switches and their heatsinks are mounted flat on top of the DC bus capacitors, while the filter components are mounted below the DC bus. Evident in the foreground are the isolation transformers supplying the load resistors.

A close-up view of the SSC is seen in Figure 6-3, where the two three-phase modules are identified and the DC bus capacitors are seen mounted below the switches.

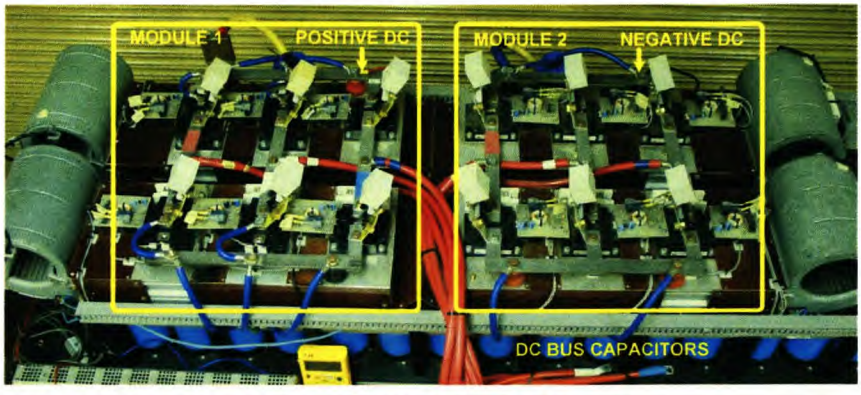


Figure 6-3: Practical SSC Configuration

A close-up view of the NPCC is seen in Figure 6-4. The two blocks identify the four switches and two diodes making up one phase-arm. Also seen is the neutral or DC centre point connection extending out from the centre of the structure.

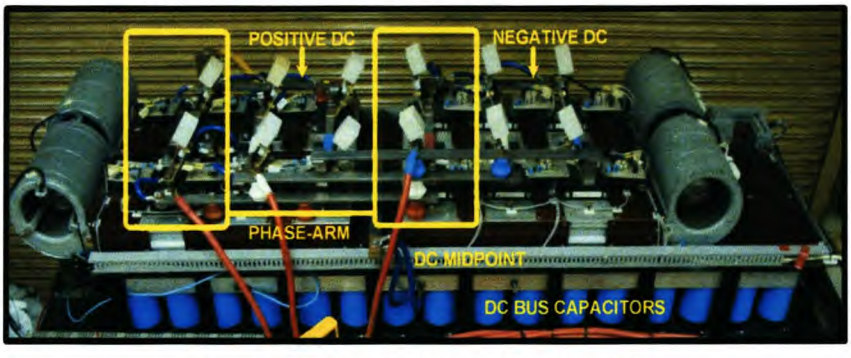


Figure 6-4: Practical NPCC Configuration

Views of the various components, required for operation and protection of the switches for

both topologies, are seen in Figure 6-5 and Figure 6-6. In Figure 6-5 the various components on the three-phase converter module are identified.

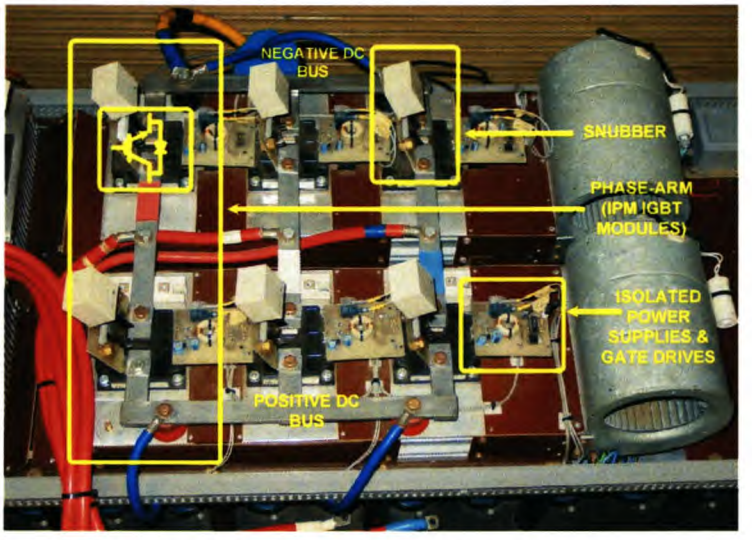


Figure 6-5: Single SSC Module with Components Identified

The isolated power supply and gate drives, specified in Table 7, are identified in the figure. A high-frequency supply is electrically isolated (3 kV) via the ferrite toroidal transformer seen on the PCB board. On the secondary side the high-frequency supply is rectified and regulated to a DC voltage of 15 V, used to power the gates of the IGBTs and supply the optical transmit and receive packages on the PCB. Over-current conditions are detected by the intelligent switch modules and an error signal is sent back to the controller via fibre optic cable. The gating signals are also received via fibre optic, ensuring that system noise does not result in incorrect operation. The over-voltage snubbers, also seen in the figure, are connected between the collector and emitter of the IGBT. They prevent over-voltage spikes from damaging the switches. More of their operation is discussed later in this chapter. A single phase-arm and the DC bus polarity are also identified in the figure.

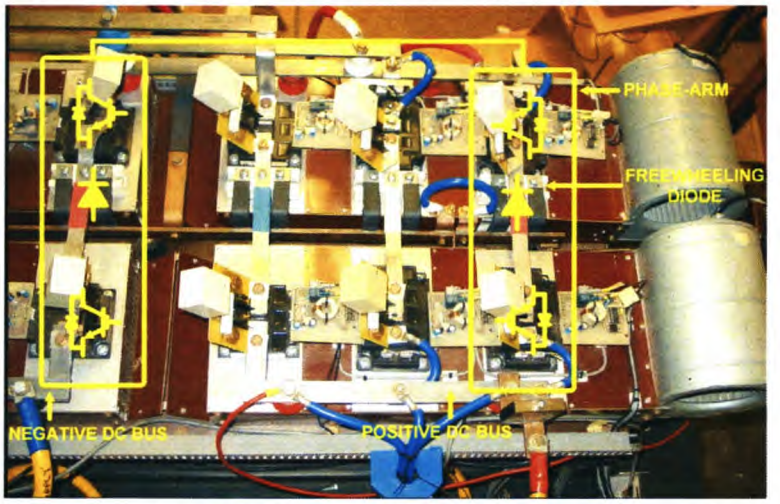


Figure 6-6: NPCC Phase-Arm with Components Identified

In Figure 6-6, a complete phase-arm is identified, made up of four switches and two free-wheeling diodes. The neutral point, connecting the diodes to the capacitor centre point is also

seen running between the IGBT heatsinks and out towards the top of the picture. The relative DC bus polarities are also indicated.

6.2.2 Converter Control

An in-house developed DSP/FPGA based controller known as the PEC31 controls the reconfigurable converter. It is equipped with a DSP, an FPGA, onboard RAM, analog to digital converters (A/D), a digital to analog converter (D/A) and numerous configurable input and output pins. The A/Ds are used for measurements, while the D/As enable digital values and commands to be written out as an analog value. The DSP is tasked with analysing measurements and states, calculating the relevant duty cycles and sending them to the FPGA. The FPGA executes the commands to the converter, adding the necessary dead time to the gating pulses. Dead time is defined as the time between switching off one switch and sending the gating pulse to its complementary switch. This is done to prevent the switches short-circuiting the DC bus.

The PEC31 controller also interfaces with a debug box, allowing messages and measurements to be written to an LCD, while receiving push button inputs from the same box. The PWM signals, calculated for the relevant switches, are sent to an optical interface board, where the electrical signals are converted into optical signals and sent optically to the converter switches. The optical board is also responsible for converting received optical error signals into electrical signals and sending them back to the PEC31 controller. The PEC31 and optical board are shown in Figure 6-7.

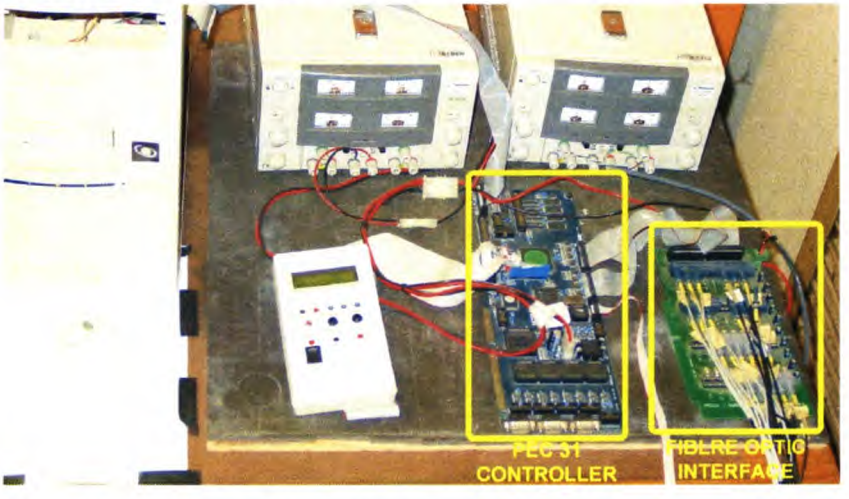


Figure 6-7: PEC31 Controller and Optical Interface Board

The converter switching code, written in C, is downloaded to the controller via a computer parallel port. The relevant codes for normal, interleaved and 3-Level SVM are listed in Appendix C. The control code for the PEC31 makes use of a number of pre-written header files, written to aid the user. Operation of the NPCC using 3-level SVM requires a different FPGA routine to be used as the gating pulses are generated differently. The routine is listed in Appendix D. Using the PEC31 controller and the relevant codes and routines listed in the ap-

pendices the converter is switched using the parameters set out in Table 8

Table 8: Practical Converter Operation Parameters

Parameters	SSC Values	NPCC Values
DC Voltage	800 V	800 V
Modulation index	0.8	0.8
Load resistance	1.8 Ω (Aϕ), 1.64 Ω (Bϕ), 1.8 Ω (Cϕ)	1.8 Ω (Aϕ), 1.64 Ω (Bϕ), 1.8 Ω (Cϕ)
Switching frequency	6 kHz	6 kHz
Switching technique	Normal and Interleaved SVM	3-Level SVM

6.3 Measurement of IGBT Operation

6.3.1 Investigation Criterion

The aim of this investigation is to gain insight into the operational behaviour of the switching within the NPCC and SSC topologies. Concerns are the overshoot on the IGBT switches and transient behaviour during switching. Investigation of the overshoot in switch voltage is performed to determine the magnitude of the parasitic inductive elements that occur between the DC bus and the switches. These parasitic impedances are particularly troublesome as they can lead to destruction of the switches. With the same converter unit being re-configured for both the SSC and NPCC, the parasitic components are expected to be the same.

To evaluate the effectiveness of the snubber used, a simulation was performed of a switch operating with the snubber excluded and thereafter included. The simulation uses a switch model whose characteristics are based on the data obtained from the IGBT datasheets and simulation package information on the modelling requirements. The simulation model of the switch, along with its switch turn-on and output characteristics, is seen in Figure 6-8. Also displayed is the snubber circuit and its component values.

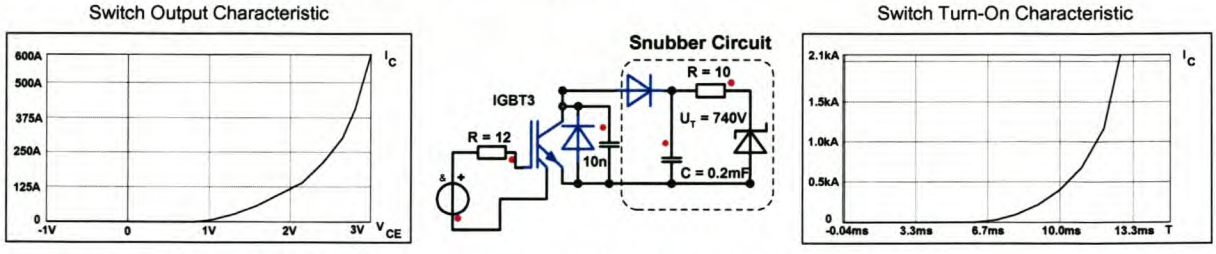
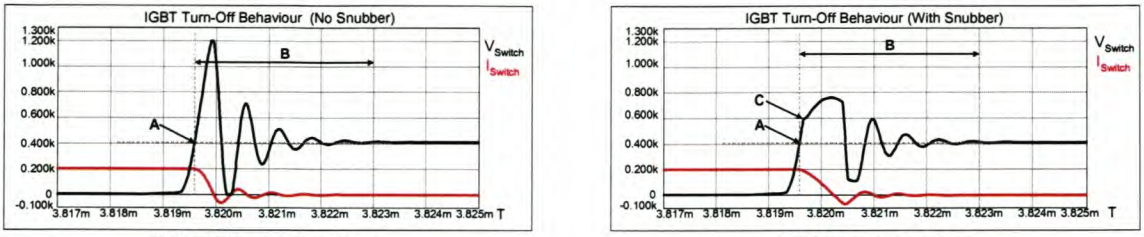


Figure 6-8: Simulation IGBT Switch Model and Snubber Circuit (IGBT Characteristics Included)

Figure 6-9(A) shows switch operation without a snubber for a parasitic inductance of 900 nH. The voltage overshoot is slightly larger than 1200 V. The mechanism causing this effect is as follows. As the switch turns off, it continues to conduct until it has reached the DC bus voltage, point A in Figure 6-9(A). Thereafter the current starts to decay, the energy stored in the parasitic inductive elements delaying the action. This *di/dt* and the parasitic impedance result in the voltage spike over the switch. The disturbance in the voltage and current waveforms, seen in period B in Figure 6-9(A), is a result of oscillation that occurs between the parasitic inductance and the collector-emitter capacitance of the IGBT, modelled as 10 nF.

This condition is highly undesirable since the IGBT voltage ratings are 1200 V, and switch destruction will occur.



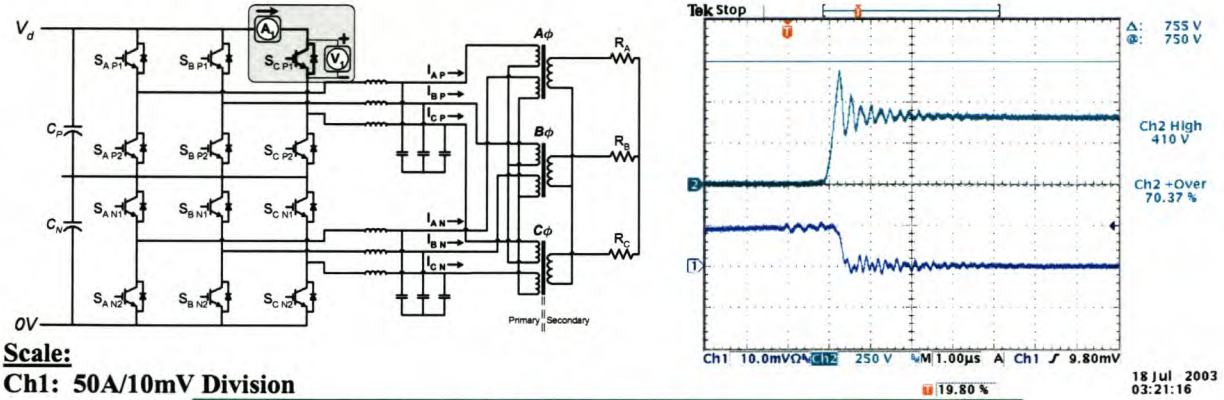
(A) Without Snubber **(B) With Snubber**

Figure 6-9: Simulated Voltage Overshoot

The snubber performs voltage clamping by making use of a diode, a capacitor, a resistor and a tranzorb. As the voltage of the spike exceeds the capacitor voltage, the diode is forward biased and the energy causing the spike is dissipated into the capacitor. The tranzorb, selected to start conducting at 740 V, is placed in parallel with the capacitor. As the capacitor voltage rating exceeds the tranzorb's conduction setting, the capacitor discharges through the resistor into the tranzorb, dissipating the energy of the spike. As the voltage drops to the conduction level of the tranzorb, the current through the resistor ceases to flow. Snubber operation, seen in Figure 6-9(B), indicates marker C as the point at which the energy of the overshoot is dissipated. Snubbers were thus fitted to the switches of the re-configurable converter, in order to prevent any destruction as a result of voltage overshoot.

The second part of the investigation involves the switch behaviour during operation. For this investigation, each topology is investigated separately.

6.3.2 Switching behaviour for the SSC



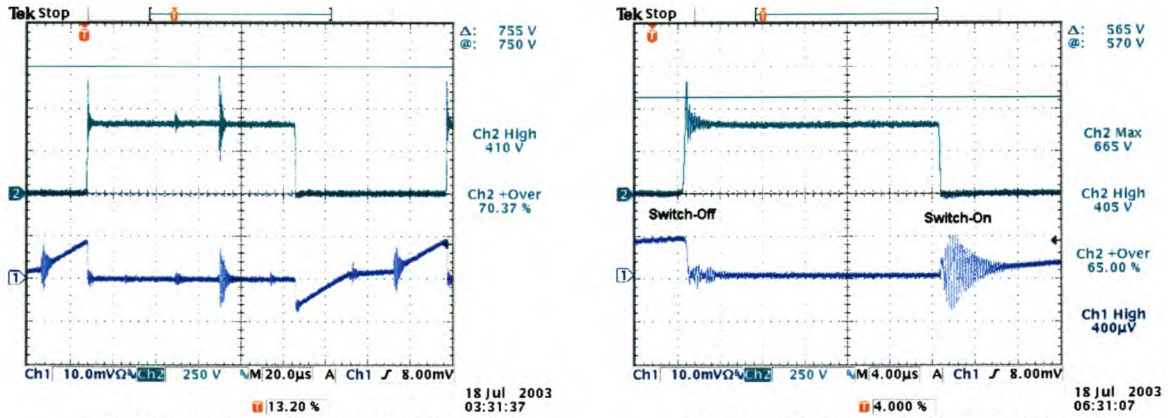
Scale:
Ch1: 50A/10mV Division

Measuring Point	Measured Value	Channel on Scope	Description
A_1	I_{SWITCH}	Ch 2	Cϕ Switch Current
V_1	V_{SWITCH}	Ch 1	Current through Switch S_{CP1}

Figure 6-10: Switch Behaviour and Measurement Points for the SSC (Switch $S_{C\,P1}$)

Measurements recorded, in Figure 6-10, of the voltage and current waveforms show a switch overshoot of 410 V, a *dt* time of 200 ns and a switched current of 50 A, equating to a value of 1.15 µH for the parasitic inductance. This approximates to about 57 nH/cm, the

length of the conductor connecting the DC bus capacitors to the IGBTs. The oscillations between the parasitic inductances and the collector-emitter capacitance are clearly visible. In Figure 6-11, the operation of the switches during modulation can be seen. Also evident in Figure 6-11(A) are the voltage spikes seen over the switch while it is open. Some of the voltage spikes, experienced by all the open switches, are attributed to switches opening in other phase-arms.

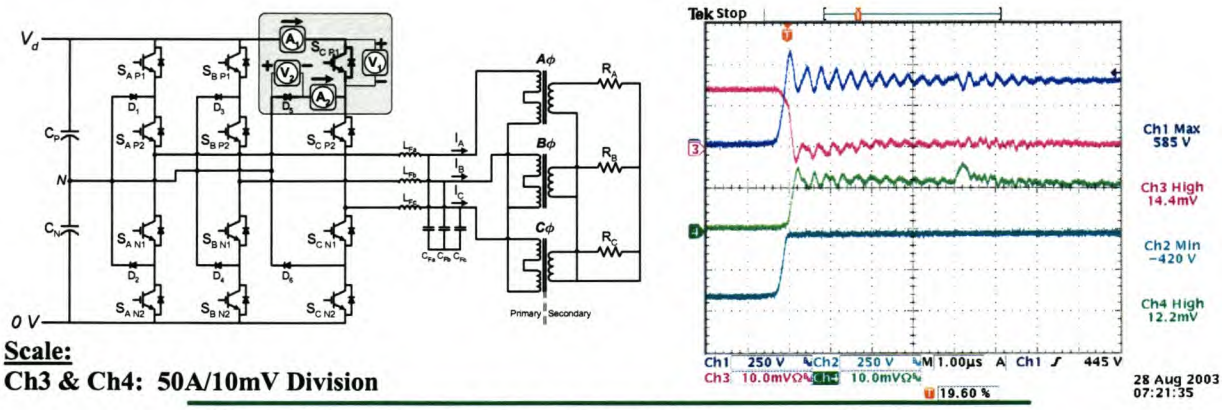


(A) Ch1 Scale: 50A/10mV Division **(B) Ch1 Scale: 50A/10mV Division**

Figure 6-11: Switching of the SSC (Switch $S_{C\,P1}$)

Voltage spikes, seen in Figure 6-11(B), are also caused during switch-on. The disturbance is caused by oscillations occurring between the switch, turning on, and the freewheeling diode of its complementary pair trying to switch off. The switch-on current oscillates between the collector emitter capacitance and the diode's parasitic components. Using single switches, as was the case for the re-configurable converter, results in these parasitic elements being present between the top and bottom switches. This is remedied by using IGBT packages with dual switches. Other observations are the switching periods, for the SSC, being 166 µs.

6.3.3 Switching behaviour for the NPCC



Scale:
Ch3 & Ch4: 50A/10mV Division

Measuring Point	Measured Value	Channel on Scope	Description
V_1	$V_{S\,CP1}$	Ch 1	Voltage over Switch S_{CP1}
A_1	$I_{S\,CP1}$	Ch 2	Current through Switch S_{CP1}
V_2	V_{D5}	Ch 3	Voltage over Diode D_5
A_2	I_{D5}	Ch 4	Current through Diode D_5

Figure 6-12: Switch Behaviour and Measurement Points for the NPCC (Switch $S_{C\,P1}$ & Diode D_5)

For the NPCC, similar parasitic inductance values causing switch voltage overshoot were measured and recorded in Figure 6-12. The measured value was 1.2 µH, with the approximated inductance per cm calculated as 60 nH/cm. Diode D_5's voltage and current waveforms were measured. The polarity of the diode voltage measurement is swopped for these tests.

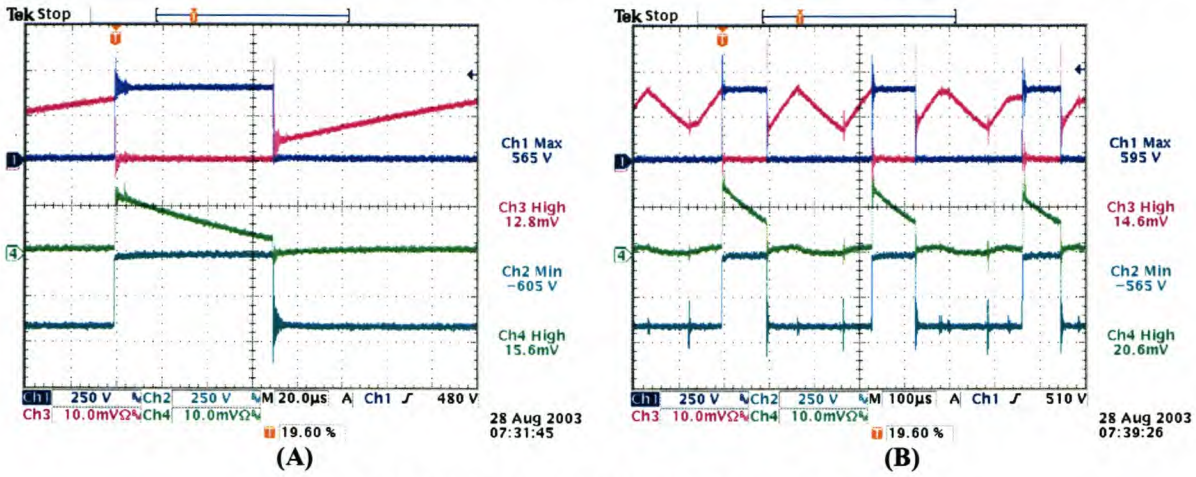
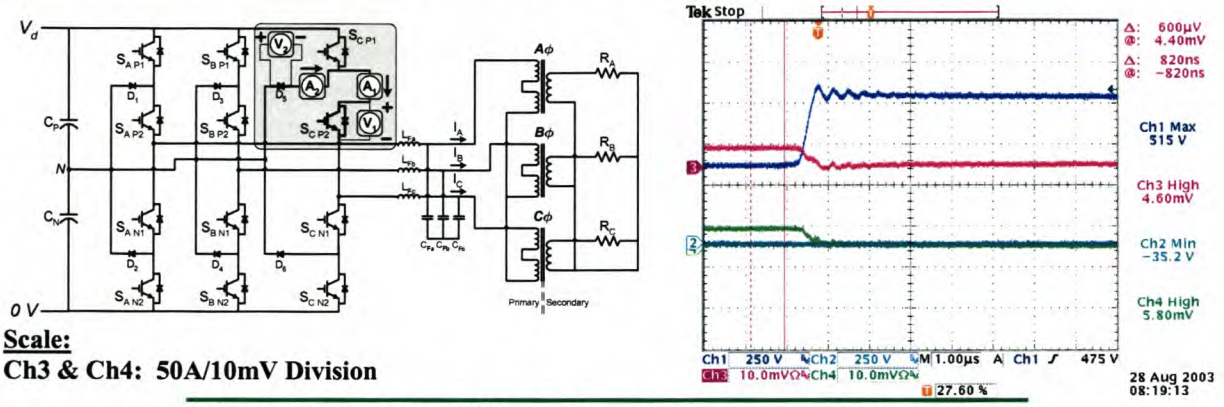


Figure 6-13: Switching of the NPCC (Switch $S_{C\,P1}$ and Diode D_5)

Also observed are the oscillations in the switch voltage and current waveforms, expected switch behaviour, as previously discussed. The interaction between switch $S_{C\,P1}$ and diode D_5 is seen in Figure 6-13(A&B). The currents show that as switch $S_{C\,P1}$ is turned off, the diode D5 becomes forward biased and starts to conduct, creating the required freewheeling current path. As switch $S_{C\,P1}$ switches on, the diode switches off, resulting in a similar voltage overshoot over the diode. This implies that the diode also requires a snubber, where parasitic components are high. Its parasitic path exists between the DC neutral point and its anode. It is thus essential that the freewheeling diodes be placed as close as possible to their relative phase-arms and the centre point of the DC bus.



Scale:
Ch3 & Ch4: 50A/10mV Division

Measuring Point	Measured Value	Channel on Scope	Description
V_1	$V_{S\,CP2}$	Ch 1	Voltage over Switch S_{CP2}
A_1	$I_{S\,CP2}$	Ch 2	Current through Switch S_{CP2}
V_2	V_{D5}	Ch 3	Voltage over Diode D_5
A_2	I_{D5}	Ch 4	Current through Diode D_5

Figure 6-14: Switch Behaviour and Measurement Points for the NPCC (Switch $S_{C\,P2}$ & Diode D_5)

An alternative observation is the 332 µs switching period for switch $S_{C\,P1}$, indicating that

its switch state stays the same for two switching periods.

Measuring the voltage and current waveforms over switch $S_{C\,P2}$ is also required, to observe its turning-off behaviour. Measurements are recorded in Figure 6-14. The overshoot measured on switch $S_{C\,P2}$ is considerably less than that observed over $S_{C\,P1}$; however, the parasitic inductance measured is 2 μH.

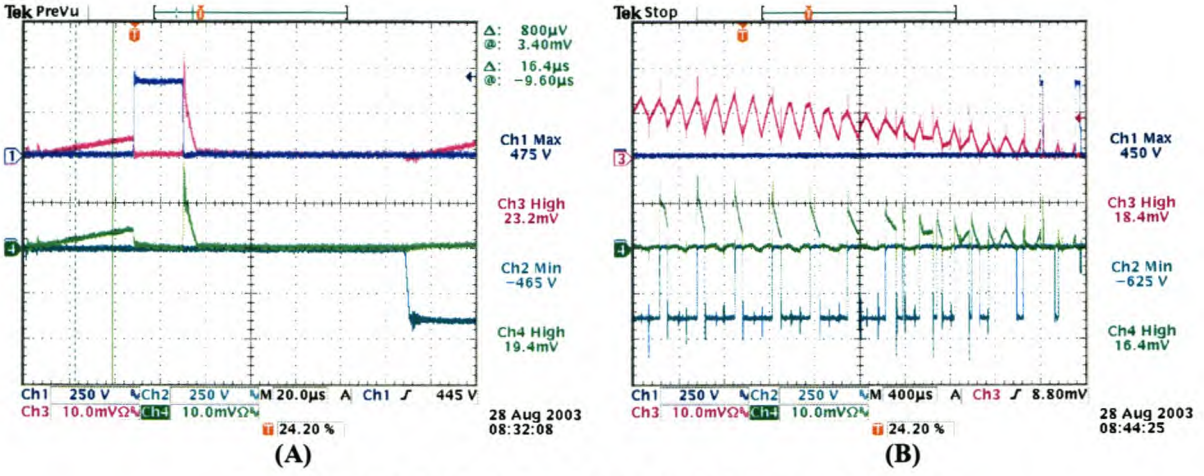


Figure 6-15: Switching of the NPCC (Switch $S_{C\,P2}$ and Diode D_5)

The parasitic path in this case is the freewheeling diode D_5's path and the distance between D_5 and switch $S_{C\,N1}$, a much longer parasitic path than for $S_{C\,P1}$. The only difference here is that the currents through the switch are usually low when turning off. This is verified in Figure 6-15(B), where the on state of $S_{C\,P2}$ is seen conducting for most of the window length. Other observations are the diode and switch turn off currents, Figure 6-15(A). After breaking the phase current, it can be seen that when $S_{C\,P2}$ turns on, freewheeling current is shared with other phase-arms.

6.3.4 Summary

By examining the switching behaviour for both topologies on the re-configurable converter, the following observations can be made:

- Reduction in parasitic inductances is essential in order to reduce the potential voltage magnitudes simulated in the discussion on the snubber operation.
- Wherever possible modular switch units should be used, ensuring the lowest possible inter switch parasitic components.
- For the NPCC, modular units containing the IGBTs and the freewheeling diode are desired.
- The switches must be placed as close as possible to the DC bus capacitors. This applies to all topologies.
- The freewheeling diode must also be placed as close possible to the capacitor centre point.

6.4 Verification of Practical Operation as an SSC and NPCC

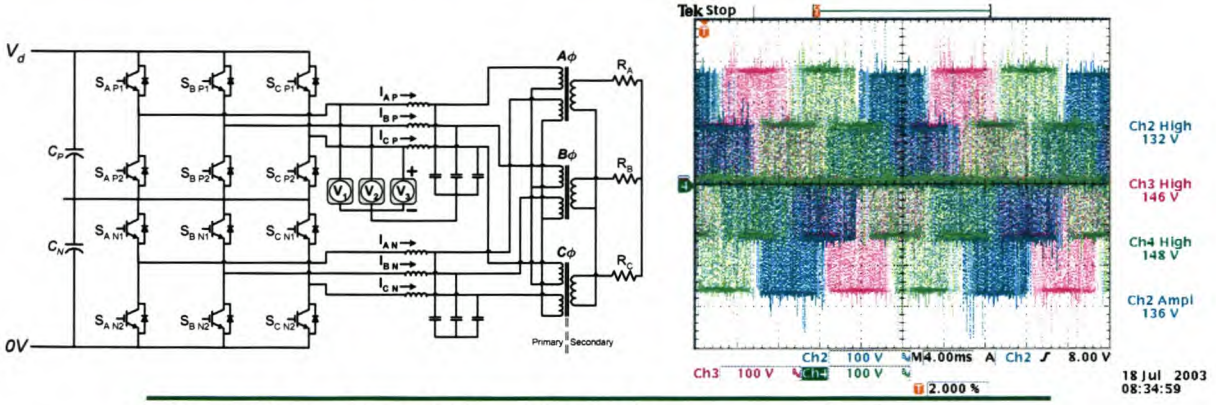
6.4.1 Converter Operation

6.4.1.1 Investigation Criterion

To verify the correct operation of the two topologies, the converters' switched DC output voltage is examined. The modulation of DC voltages, i.e. the pulse width times discussed in the previous chapter, are not the primary focus. The shapes and number of the stepped output voltage levels for the topologies are the main issues, rather than the pulse widths. The number of output voltage levels indicates the correct operation of each topology. Furthermore, the modulation techniques disallow ground connections, so the modulated DC waveforms of the three-phase converter topologies being compared cannot be measured with reference to ground, for lack of the ground connection. All measurements are measured to the star point of the filter capacitors. During switching, the modulated DC voltage of the three-phase converters, unlike that of the single-phase converters seen in Chapter 3, has a higher number of switched voltage levels due to the interaction between phase-arms. It has the same effect on the modulated DC voltages as unipolar switching does. For the SSC, five output voltage levels are expected, whereas seven output voltage levels are expected for the modulated DC voltage of the NPCC.

Verification of correct operation for the various switching modes, normal and interleaved SVM, applied to the SSC also requires that the ripple currents be compared. That being done, the current contribution from both converters, making up the SSC, to the isolation transformer needs investigation. This was measured to ensure that both converters share the load.

6.4.1.2 Practical SSC Results Using Normal SVM



Measuring Point	Measured Value	Channel on Scope	Description
V_1	$V_{A\,P\,Conv.}$	Ch 2	Top Converter's Aϕ Output Voltage
V_2	$V_{B\,P\,Conv.}$	Ch 3	Top Converter's Bϕ Output Voltage
V_3	$V_{C\,P\,Conv.}$	Ch 4	Top Converter's Cϕ Output Voltage

Figure 6-16: Modulated DC Voltage of the SSC using Normal SVM

The first of the topologies investigated is that of the SSC using normal SVM. The practi-

cal waveforms, in Figure 6-16, show all three phases, their measurement points and a 5-level output voltage waveform, a result of the measurement ground connection. The voltage steps occur in steps of approximately 140 V while operating at a DC bus voltage of 400 V, per converter unit, and a modulation index of 0.8. The overall DC bus voltage is 800 V. The key, tabulated at the bottom of Figure 6-16, ties the measured values to the measurement points in the converter schematic. The top and bottom converter outputs are identical.

The practical measurements taken on the converter required that the voltages be measured with reference to the star point of the filter capacitors. This was the only connection available as a reference. Using the simulation model enables the actual converter output voltage to be measured, while comparing the measured value to the same measurement in the model. In Figure 6-17(A) the voltages measured in Figure 6-16 are simulated. Both have voltage magnitudes of approximately 280 V, while Figure 6-17(B) shows that the actual converter ϕ-ϕ voltages are 400 V in magnitude and take the form of a 3-level stepped output voltage.

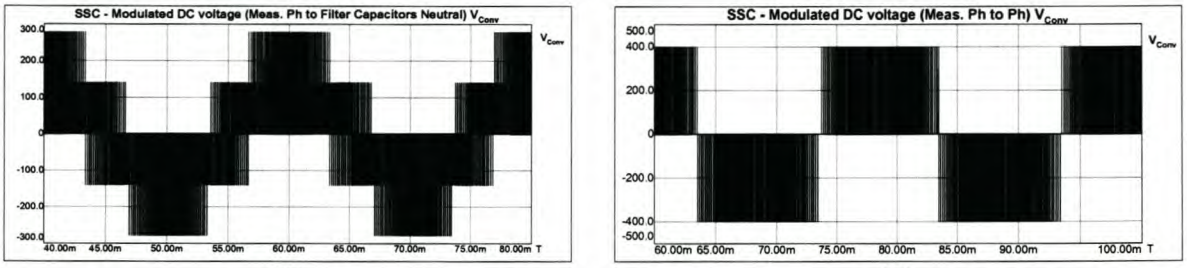


Figure 6-17: Simulated Phase-Phase Modulation of the DC Voltage for the SSC

Figure 6-18 is the measured output voltage of the Aϕ phase-arm only. An FFT of the harmonic components is shown of the high-frequency components (A) and the low-frequency (B) components of the output waveform and is expressed in dB (20Log[actual value]).

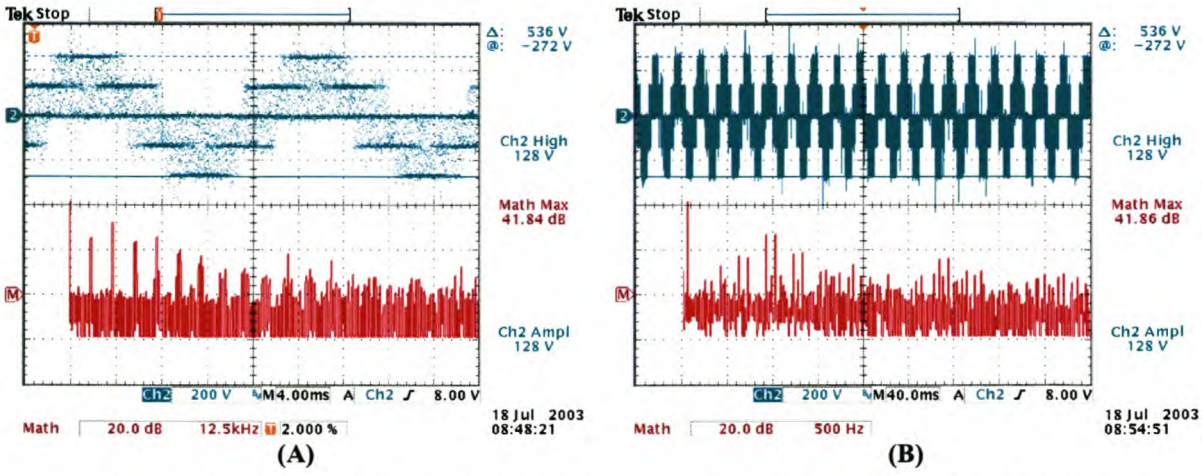
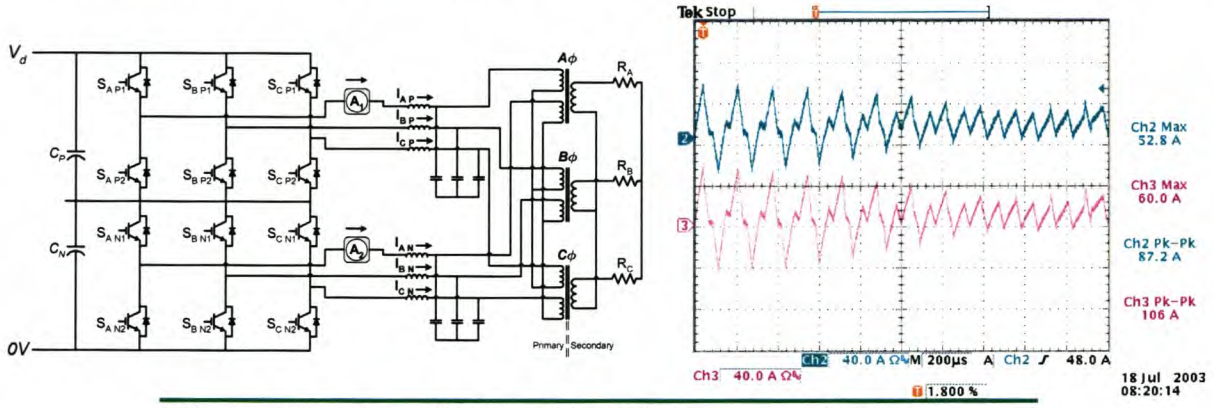


Figure 6-18: Modulated DC Voltage of the SSC using Normal SVM (A-Phase of Top Converter)

In Figure 6-18(A), where the FFT scale is set to 12.5 kHz/div, the high-frequency components, occurring at multiples of the 6 kHz switching frequency, can clearly be seen. In Figure 6-18(B), with FFT scale set to 500 Hz/div, the lower frequency components are seen. These

values serve to provide information for designing the low-pass filters and, as can be seen in the figure, start in the region of 250 Hz, with the larger components found from 400 Hz onwards. It should be noted that the lower frequency components are a result of the loading, so as loading changes the harmonics will change.

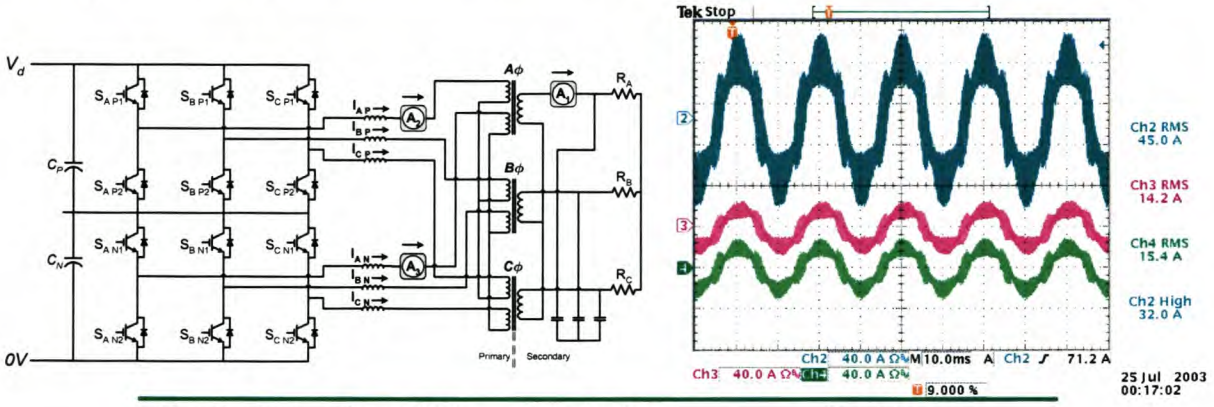
The parallel gating of the two converters stacked in series is only apparent when measuring the output current from both top and bottom converters. Current measurement also provides the necessary measurement isolation between the two converters, operating at different voltage levels. The combined operation of the two converter modules is confirmed by the measurements recorded and shown in Figure 6-19.



Measuring Point	Measured Value	Channel on Scope	Description
A_1	I_{AP}	Ch 2	Aϕ Top Conv. Ripple Current
A_2	I_{AN}	Ch 3	Aϕ Bottom Conv. Ripple Current

Figure 6-19: Top and Bottom SSC Current Measurements Illustrating Combined Operation (Normal SVM)

The parallel operation is thus verified by noting that the ripple currents are in phase with each other. It is possible to place the filter capacitors on the secondary of the transformer, but this requires that they be rated for the full load operation.



Measuring Point	Measured Value	Channel on Scope	Description
A_1	I_A	Ch 2	Aϕ Load Current (Transformer Sec.)
A_2	I_{AP}	Ch 3	Aϕ Load Current (Transformer Prim.)
A_3	I_{AN}	Ch 4	Aϕ Load Current (Transformer Prim.)

Figure 6-20: SSC Primary and Secondary Transformer Ripple Current Measurements (Normal SVM)

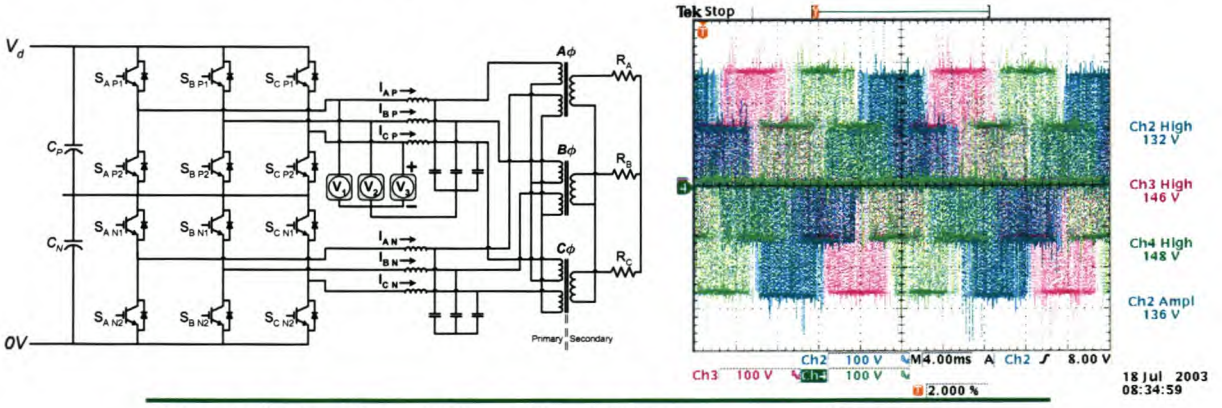
Using normal SVM, a reflection of the summated primary currents and the switching frequency ripple will be evident in the secondary current, no matter how many converters are

stacked in series. The transformer will also experience higher electrical stress than the current configuration, due to the eddy current and iron core losses from the switched ripple current.

Moving the filter capacitors to the secondary side of the transformer, the abovementioned phenomenon is observed. In Figure 6-20 the summated secondary ripple current is observed. The primary ripple currents from both converters, which are combined in the transformer, are also seen. The transformer's winding ratio of 1:1: 0.619 results in the stepping up of the secondary currents magnitude. The current contributions from both converters are slightly different, this being attributed to the single-phase transformer units, making up the three-winding transformer, not having exactly the same impedances.

6.4.1.3 Practical SSC Results Using Interleaved SVM

The operation of the SSC, using interleaved switching, shows similar 5-level modulated DC waveforms when measuring on the converter side of the filter inductor.



Measuring Point	Measured Value	Channel on Scope	Description
V_1	$V_{A\,P\,Conv.}$	Ch 2	Top Converter's Aϕ Output Voltage
V_2	$V_{B\,P\,Conv.}$	Ch 3	Top Converter's Bϕ Output Voltage
V_3	$V_{C\,P\,Conv.}$	Ch 4	Top Converter's Cϕ Output Voltage

Figure 6-21: Modulated DC Voltage of the SSC using Interleaved SVM

Between phases the converter voltage has the same shape as that in Figure 6-17(B). The measurements in Figure 6-21 are only of the top converter module since it is only possible to measure one module at a time. The oscilloscope is limited to four channels only and ground loops pose a problem. Furthermore, the phase shifting of the top and bottom converter outputs is better viewed by looking at the currents.

Measuring the A-phase only, an FFT measurement of the harmonic components is recorded. Figure 6-22(A), measured at 12.5 kHz/div indicates that high-frequency components occur at similar intervals to those of the normal SVM converter. It is expected as the top module is operating as a normal three-phase converter using 2-level SVM. Thus the harmonic spectrum is similar to that of the previous case. Figure 6-22 (B) is a measurement of the low-frequency components in the waveform, also similar to the previous case.

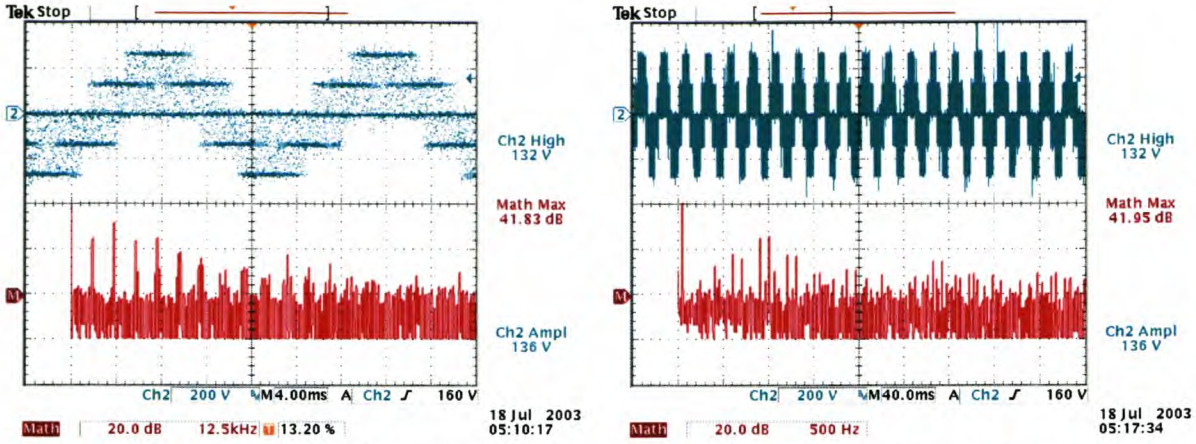
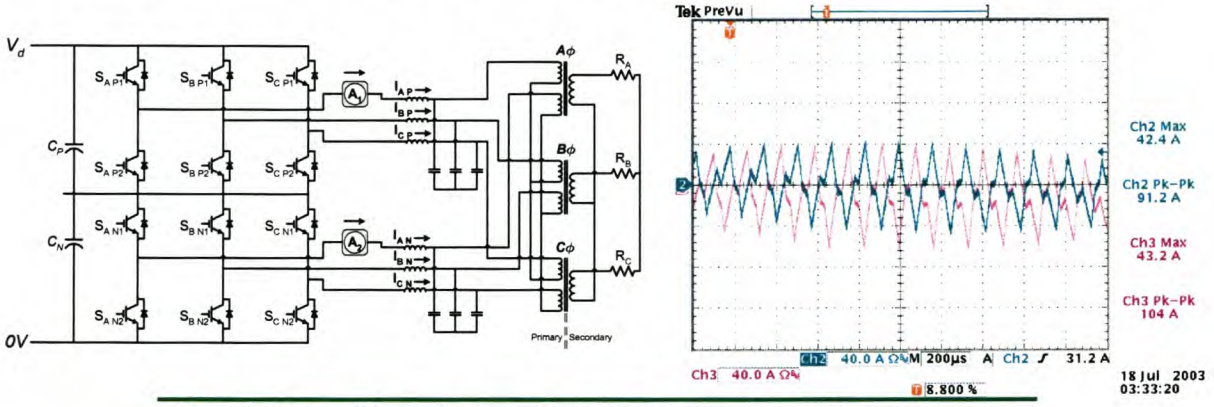


Figure 6-22: Modulated DC Voltage of the SSC using Interleaved SVM (A-Phase of Top Converter)

The interleaved SVM switching is apparent in Figure 6-23, where the top and bottom converter ripple currents are compared. The 180° phase shift in the gating pulses between the top and bottom converters is seen in the measured currents.

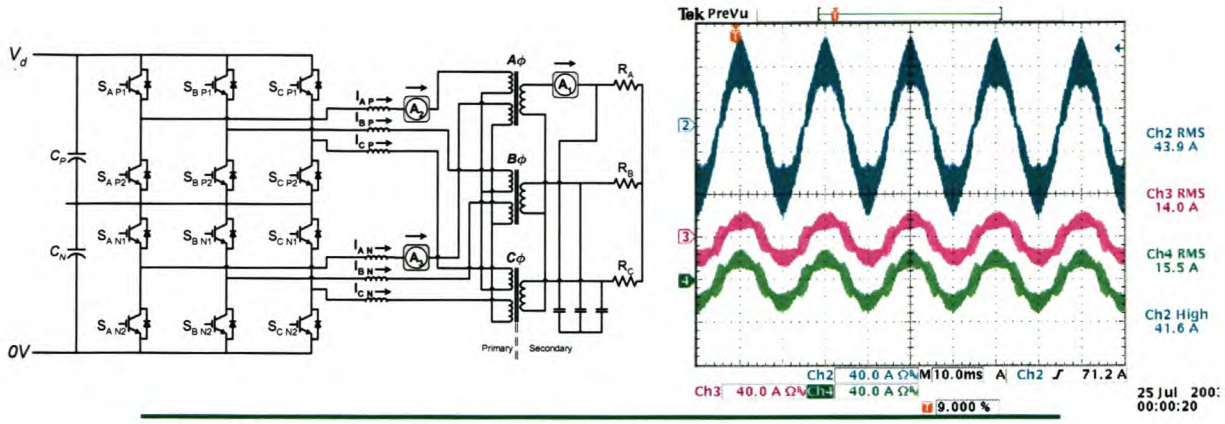


Measuring Point	Measured Value	Channel on Scope	Description
A_1	I_{AP}	Ch 2	Aϕ Top Conv. Ripple Current
A_2	I_{AP}	Ch 3	Aϕ Bottom Conv. Ripple Current

Figure 6-23: Top and Bottom SSC Current Measurements Illustrating Combined Operation (Interleaved SVM)

Placing the filter capacitors on the secondary side of the transformer, the primary side currents and load side current of the A-phase are measured and shown in Figure 6-24.

The load side current in Figure 6-24 clearly has a lower current ripple component than that measured for the SSC using normal SVM. Accurate measurements of these values, performed later in this chapter, evaluate the extent of the difference. Also evident is that the contributing currents on the primary side of the transformer are similar to those of the previously mentioned case. Using interleaved switching results in the secondary current of the summated primary currents to naturally contain less low switching frequency harmonics. It also ensures that the transformer experiences less stress because of the distributed ripple currents. Unlike normal SVM operation, the higher the number of series converter modules in the SSC using interleaved switching, the lower the ripple currents. This makes it possible omission of the filter capacitors. This results in a reduction in the filter capacitor component count.

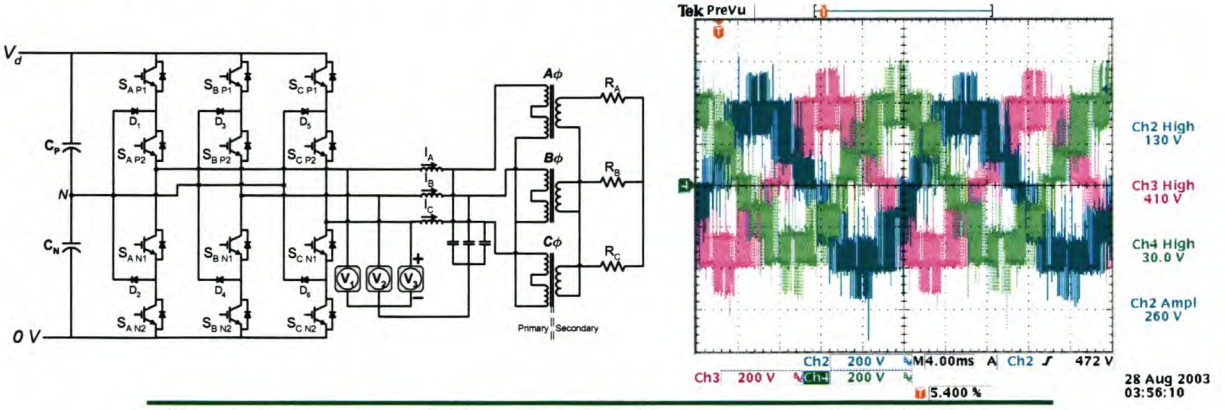


Measuring Point	Measured Value	Channel on Scope	Description
A_1	I_A	Ch 2	Aϕ Load Current (Transformer Sec.)
A_2	I_{AP}	Ch 3	Aϕ Load Current (Transformer Prim.)
A_3	I_{AN}	Ch 4	Aϕ Load Current (Transformer Prim.)

Figure 6-24: SSC Primary and Secondary Transformer Ripple Current Measurements (Interleaved SVM)

6.4.1.4 Practical NPCC Results Using 3-Level SVM

Unlike that of the SSC topologies, the NPCC topology's modulated DC output voltage, measured in the same manner as that of the SSC, yields a 9-level output like that displayed in Figure 6-25 and simulated in Figure 6-26(A). The voltage between converter phase-arms is a 5-level output voltage waveform like that simulated in Figure 6-26(B). As explained in Chapter 4, this is made possible by the three distinct states that each phase-arm is capable of being switched into, namely the positive, negative and zero states. Like the SSC, interaction similar to that of unipolar switching occurs between the three phase-arms.

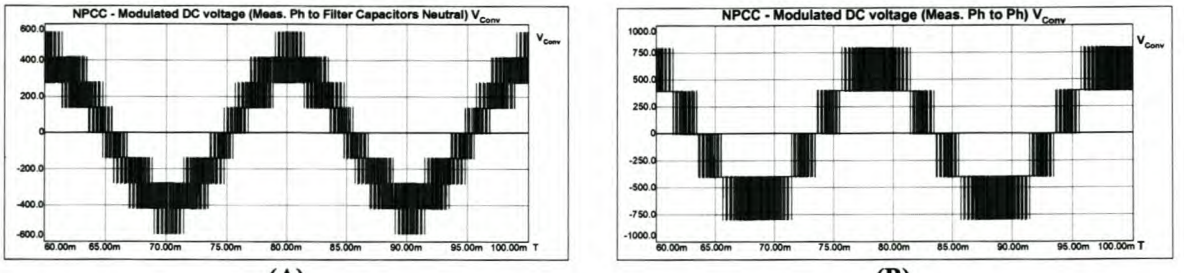


Measuring Point	Measured Value	Channel on Scope	Description
V_1	$V_{A\ Conv.}$	Ch 2	Top Converter's Aϕ Output Voltage
V_2	$V_{B\ Conv.}$	Ch 3	Top Converter's Bϕ Output Voltage
V_3	$V_{C\ Conv.}$	Ch 4	Top Converter's Cϕ Output Voltage

Figure 6-25: NPCC Output Voltage Measurements

For the NPCC the stepped voltage has steps of approximately 160 V when operating with a DC bus of 800 V and a modulation index of 0.8. The primary differences are that the waveforms peak at approximately 550 V, and have peak-peak amplitudes of approximately 1100 V. This is possible since the converter has the ability to reverse the polarity of the DC

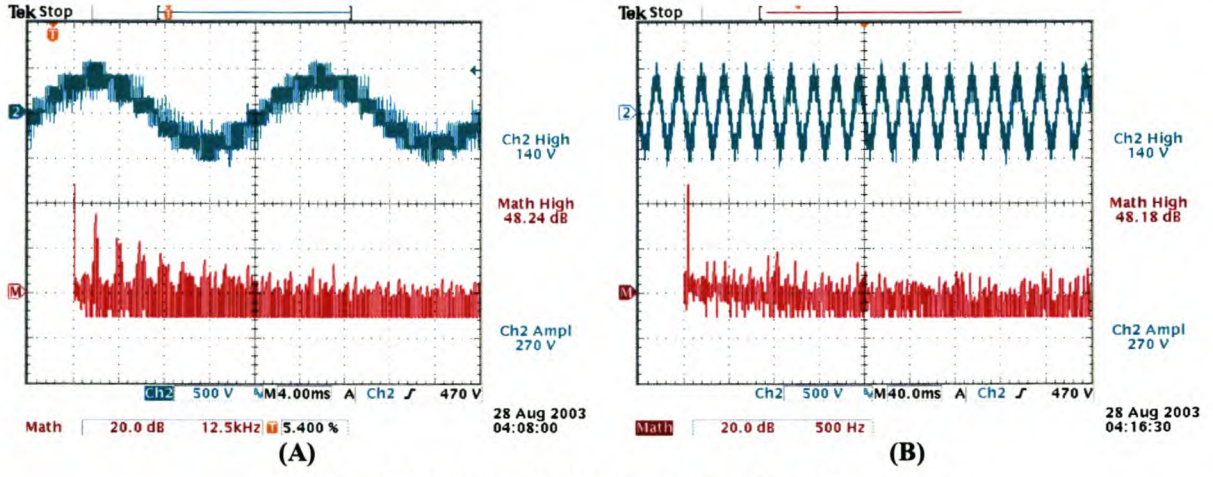
voltage applied to the inductor.



(A) (B)

Figure 6-26: Simulated Phase-Phase Modulation of the DC Voltage for the NPCC

Figure 6-27 provides information as to the frequency components by measuring the A-phase exclusively. The high-frequency components, Figure 6-27(A) with an FFT taken at 12.5 kHz/div, occur in multiples of the 6 kHz switching frequency. The lower frequency component measurements are observed in Figure 6-27(B). The measurement is performed to determine load impact on the waveforms.



(A) (B)

Figure 6-27: Modulated DC Voltage of the NPCC (A-Phase)

6.4.1.5 SSC and NPCC Topological Assessment

Measuring and examining the various converters' modulated DC output waveforms, the following observations can be made:

- Firstly, the stepped output voltages and the number of voltage levels measured confirm the correct practical operation of each of the topologies.
- The steps of 140 V for the SSC and 160 V for the NPCC ensure that the filter inductors are not exposed to high *dv/dt's*, thereby reducing the electrical stress.
- The SSC measurements of the transformer primary currents confirm the sharing of the load by both top and bottom units.
- Practical interleaved switching of the SSC is observed and the benefit, i.e. the decrease in the output ripple current, is evident in the measurements.

6.5 Performance of Various Switching Schemes

6.5.1 Investigation Criterion

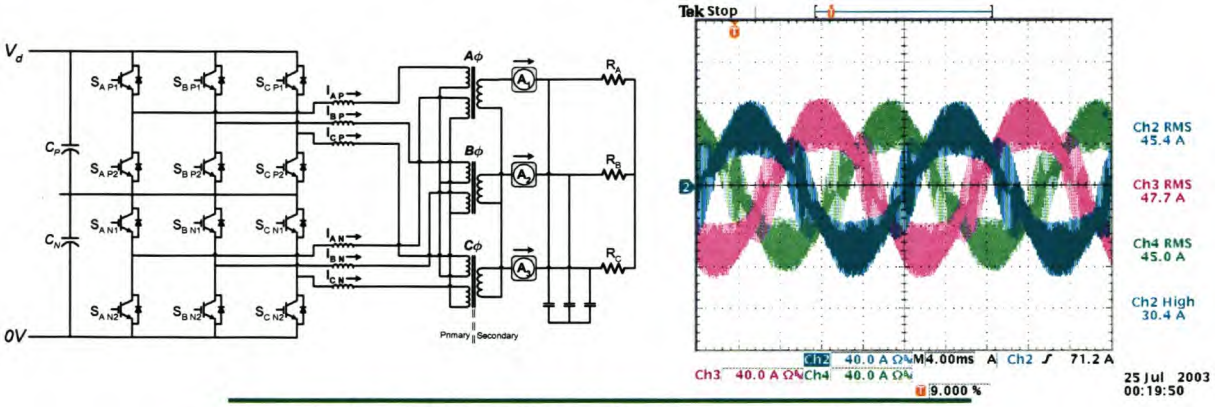
Investigation of the unfiltered load current quantities provides insight into the multilevel converter performances, specifically the performance of the control techniques, i.e. the normal 2-level SVM, the interleaved 2-level SVM and the 3-level SVM. Using open-loop switching, a performance comparison between the modulation strategies can be performed. Load currents before the filter capacitors, after the filter capacitors, and the output voltage waveforms are considered.

A comparison between the load voltages of the topologies with the transformer in and out of the circuit is also performed. In order to test the switching technique for the SSC, the topology requiring the transformer, the output of one of the series stacked converters is applied to a balanced transformer-less load. Switching the NPCC and one module of the SSC into the identical resistive load at a reduced DC bus rating ensures that the transformer non-idealities do not affect the evaluation of the topologies.

6.5.2 Unfiltered Load Current Waveforms (Transformer Secondary)

Measuring the unfiltered load current of the topologies, i.e. before the filter capacitors, facilitates the measurement of the switching frequency components on the load side of the transformer. For the SSC, the benefit of using interleaved SVM is only apparent after the two output currents are summated within the transformer. These measurements can be compared to the normal SVM operation to obtain information on the ripple reduction, using interleaved SVM. Measurement of the current waveforms before the filter capacitors also provides information about any potential waveform deformation, in either the SSC or NPCC topologies.

6.5.2.1 Practical Performance of SSC Using Normal SVM



Measuring Point	Measured Value	Channel on Scope	Description
A_1	I_A	Ch 2	Aϕ Load Current
A_2	I_B	Ch 3	Bϕ Load Current
A_3	I_C	Ch 4	Cϕ Load Current

Figure 6-28: SSC Load Current Measurements – Before Filter Capacitors (Normal SVM)

The unfiltered current measurements recorded in Figure 6-28, measured at the points indicated in the figure, show the three-phase load currents with magnitudes of approximately 80 A_{peak}. Apparent is the extent of the high-frequency ripple current at zero crossing, a consequence of the counter Emf of the load being low this time. While the counter Emf is low, a large differential voltage is present over the filter inductor, resulting in a large *di* magnitude.

Evident too are the large ripple current components on the crest of the waveform, where the peak values appear to be limited by the crest shape, yet not so below the crest. This is once again a result of the counter Emf. As the current reaches its peak value, the counter Emf also reaches its peak value. With a low differential voltage over the inductor, a low *di* is experienced. As the converter switches into its freewheeling state, the converter driving voltage becomes negative, and a sharp negative *di* occurs in the ripple current, seen in Figure 6-28. This phenomenon is typical of resistive loads. If the load was inductive or capacitive, the incidence of the high-frequency ripple current components would be different, i.e. phase shifted. For the SSC, operating in this fashion, both the transformer and filter inductors would be exposed to this ripple current, the impact of which will become evident later in this chapter.

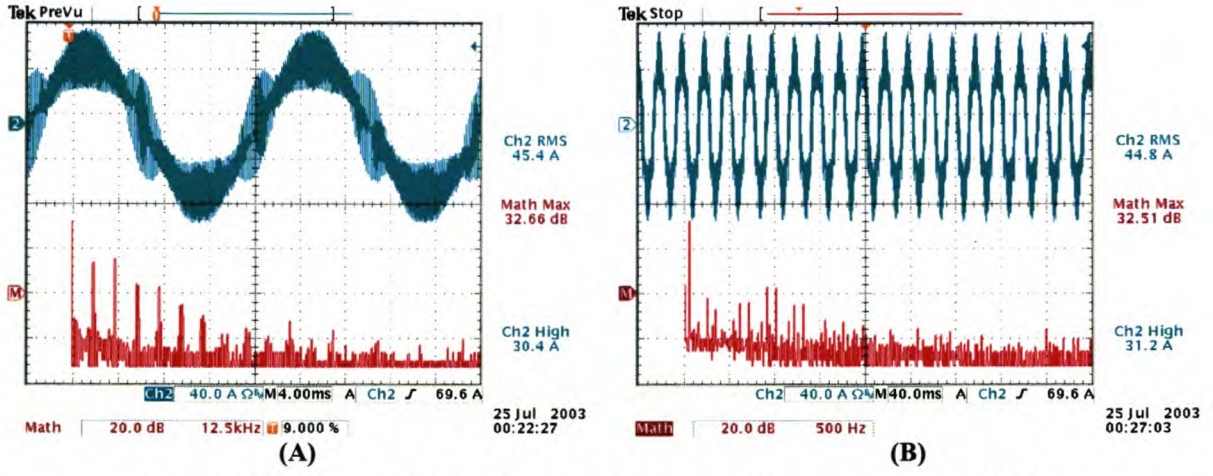


Figure 6-29: A-Phase SSC Ripple Current Frequency Components (Normal SVM)

In the record of the frequency components of the load-side ripple current, the high and low-frequency components in Figure 6-29, it is the high-frequency component incidence that requires investigation. The low-frequency components are discussed in the next section.

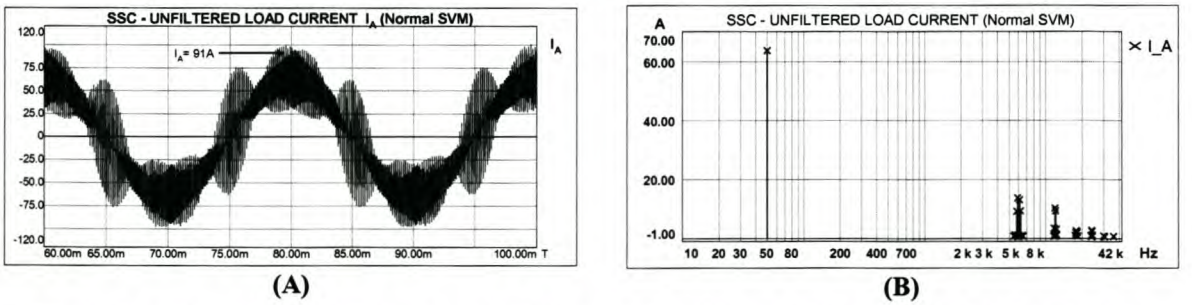
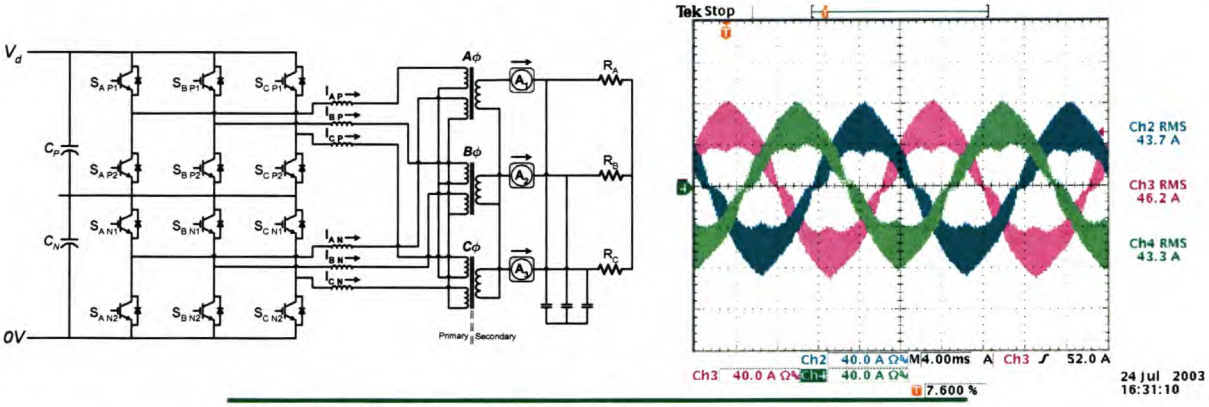


Figure 6-30: Simulated Unfiltered Load Current and FFT Components for the SSC (Normal SVM)

In Figure 6-29(A), an FFT measurement, recorded at 12.5 kHz/div, of the high-frequency components is shown. The switching frequency harmonics, occurring in multiples of the 6 kHz switching frequency, are clearly visible. An FFT, Figure 6-29(B), recorded at 500 Hz/div, shows that there is no evidence of any switching ripple at half the switching frequency. The high-frequency ripple current harmonics are recorded in Table 9. The simulated results, Figure 6-30, yield results with ripple currents similar in magnitude.

6.5.2.2 Practical Performance of SSC Using SVM Interleaved SVM

The benefit of using interleaved SVM on the SSC is evident when looking at the measured current ripple waveforms of Figure 6-31. The largest variation observed is that the ripple current magnitudes are considerably less. At the zero crossing of each waveform, the ripple current magnitudes are small compared to the SSC using normal SVM. The impact of interleafing on the measured current is best explained by considering Figure 6-32.

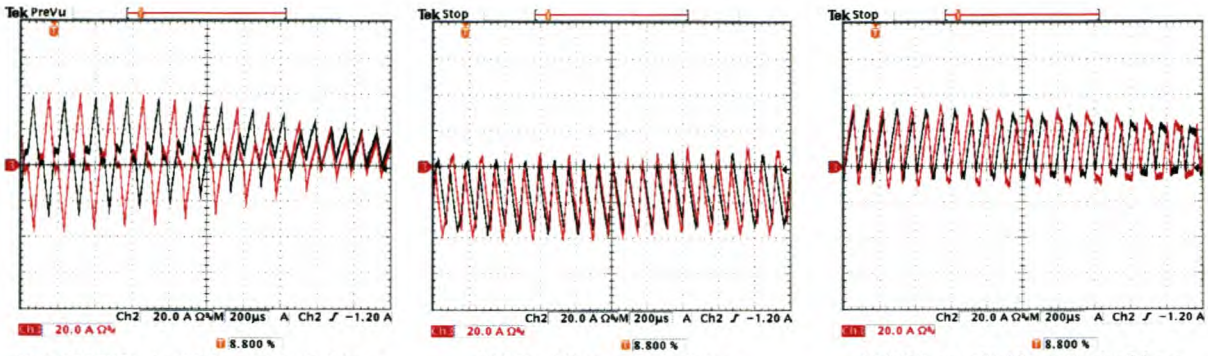


Measuring Point	Measured Value	Channel on Scope	Description
A_1	I_A	Ch 2	Aϕ Load Current
A_2	I_B	Ch 3	Bϕ Load Current
A_3	I_C	Ch 4	Cϕ Load Current

Figure 6-31: SSC Load Current Measurements – Before Filter Capacitors (Interleaved SVM)

Phase shifting of the gating pulses is expected to introduce a 12 kHz switching ripple. However this is not seen at the zero crossing. This occurrence is attributed to the application of SVM using symmetrical PWM, discussed in Chapter 4. Three effects can be observed in the ripple current waveform, namely 180° out of phase switching, in phase switching and out of phase switching. During the zero crossing region the duty ratios are typically in the region of 50%. Combined with the half a switching period delay for one of the converter modules, the result is a near cancellation of the ripple current components within the transformer. The 180° out of phase switching waveforms are seen in Figure 6-32(A).

However, as the current slope of the fundamental rises, the duty ratios change. The duty ratios reach values where the delay causes the switched currents to be perfectly in phase, like those seen in Figure 6-32(B). NNN→PNN→PPN→PPP→PPN→PNN→NNN is a typical symmetrical PWM switching sequence, where the P or N states of the switches are specified in the ABC format.



(A) 180° Out of Phase Switching **(B) In Phase Switching** **(C) Phase Shifted Switching**

Measuring Point	Measured Value	Channel on Scope	Description
A_1	I_{AP}	Ch 2	Aϕ Top Conv. Ripple Current
A_2	I_{AN}	Ch 3	Aϕ Bottom Conv. Ripple Current

Figure 6-32: Three-Phase Interleafing Effect for the SSC

While the A-phase remains in the P-state for most of the switching sequence, the phase-shifted converter follows the same sequence half a switching period later and coincides with the PPP→PPN→PNN→NNN part of the other converter. Since the PPP and NNN states are both zero states and have the same net effect on the inductor current, the converter's A-phases appear to be switching in phase with each other. The B-phase currents do not experience this effect at the same instant, but will at other stages in the fundamental period. This phenomenon results in a 6 kHz current harmonic being present in the waveform. For the remainder of the fundamental period, a 12 kHz switching ripple harmonic is expected, as the contributing currents take the form seen in Figure 6-32(C).

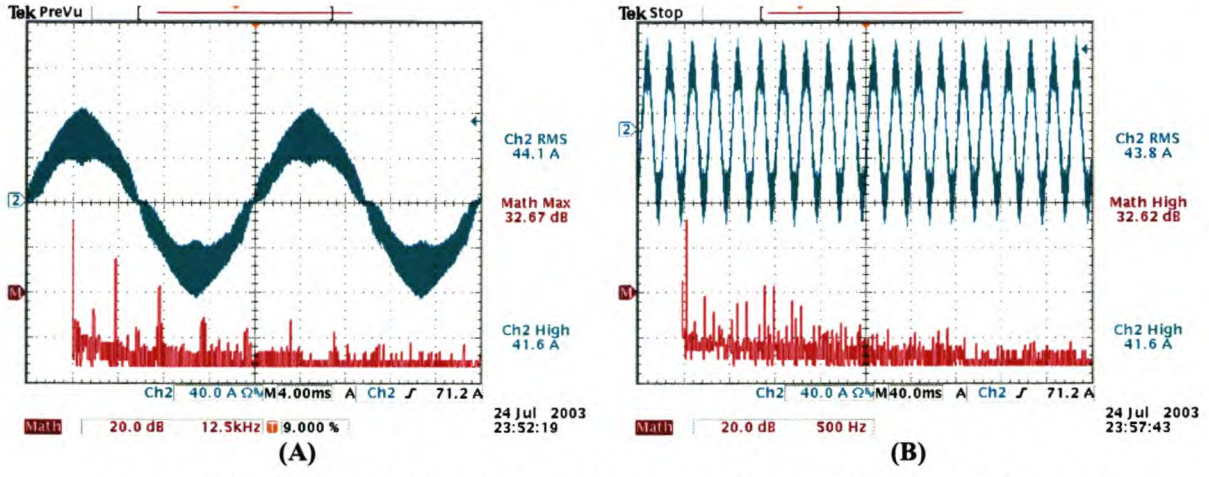
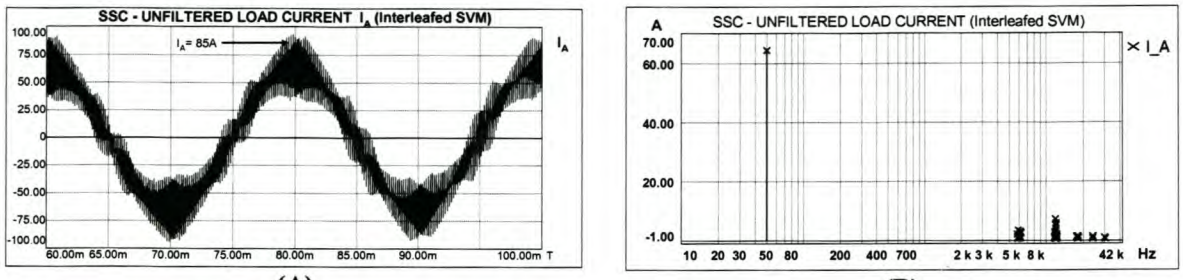


Figure 6-33: A-Phase SSC Ripple Current Frequency Components (Interleaved SVM)

The FFT performed on the ripple current, Figure 6-33, of one of the phase-arms confirms this. The measured high-frequency components, Figure 6-33(A), show the presence of a reduced 6 kHz component, when compared to the SSC operating with normal SVM. The largest current harmonic measured was that of the 12 kHz component, and multiples of itself.

The FFT measurements of the low-frequency components, Figure 6-33(B), show no presence of lower than 6 kHz components. The high-frequency ripple current harmonics, for the

SSC using interleaved switching, are also recorded in Table 9.



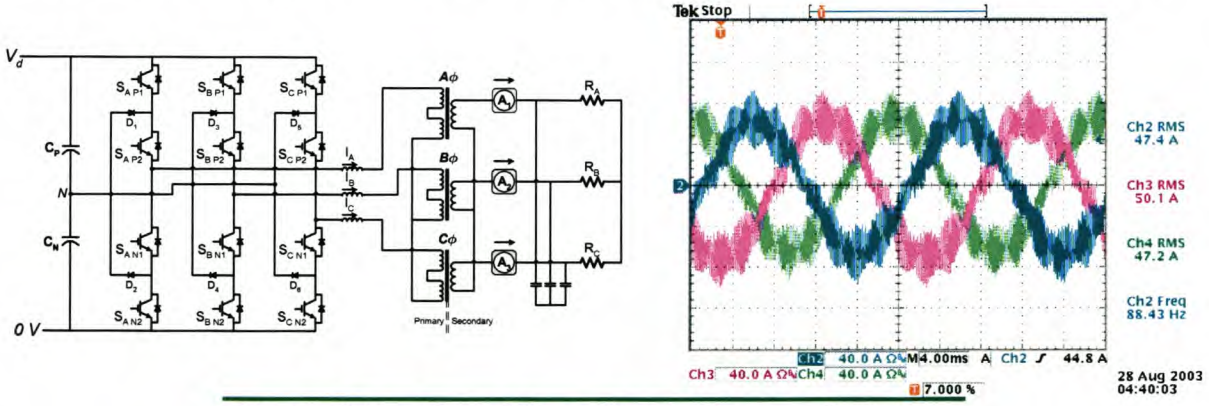
(A) (B)

Figure 6-34: Simulated Unfiltered Load Current for the SSC and FFT Components (Interleaved SVM)

The simulated waveforms, Figure 6-34, serve to provide confirmation of the frequency components measured on the practical SSC. FFTs of the simulated current also indicate the frequencies of the switching harmonics. The harmonic incidence coincides with theoretical and practical observations, with dominant components occurring at multiples of the switching frequency.

6.5.2.3 Practical Performance of NPCC Using 3-Level SVM

The three-phase ripple currents of the NPCC are measured and displayed in Figure 6-35.



Measuring Point	Measured Value	Channel on Scope	Description
A_1	I_A	Ch 2	Aϕ Load Current
A_2	I_B	Ch 3	Bϕ Load Current
A_3	I_C	Ch 4	Cϕ Load Current

Figure 6-35: NPCC Load Current Measurements – Before Filter Capacitors

As seen in the measured results, the ripple current components have less prominent amplitudes than those seen in the SSC converter. This is attributed to the 5-level modulated DC output voltages, which subject the 200 µH filter inductors to low *dv/dt*'s, resulting in lower ripple current amplitudes. The analysis of the frequency components of the ripple current in one of the phases is displayed in Figure 6-36.

The FFT measurement of the high-frequency components, Figure 6-36(A), shows harmonic components with considerably smaller amplitudes. The harmonic range is also smaller, up to approximately 36 kHz. What is observed in the NPCC, which was not seen in the SSC, is the presence of a 3 kHz component, verified in the measurement of the lower fre-

quency harmonic components, Figure 6-36(B).

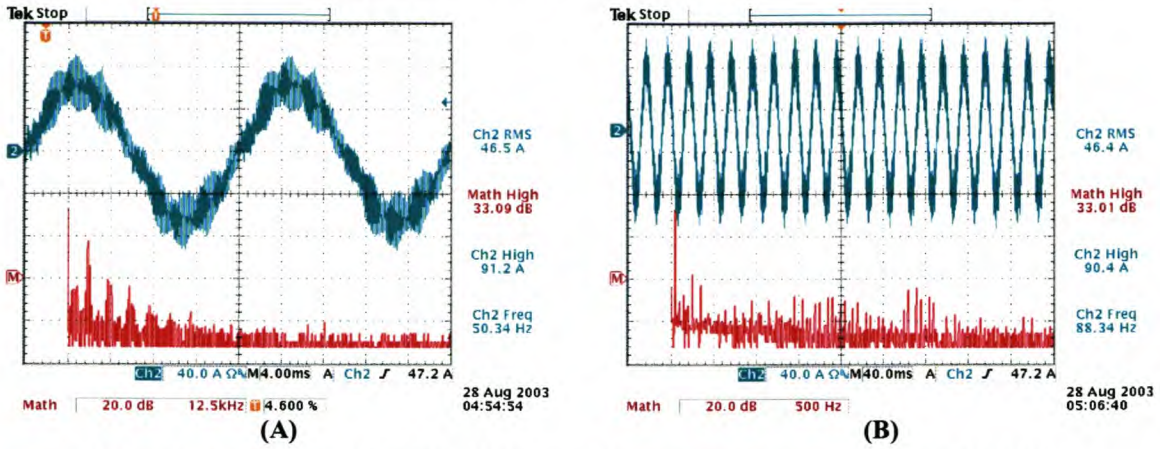


Figure 6-36: A-Phase NPCC Ripple Current Frequency Components (3-Level SVM)4

The 3 kHz components are a typical phenomenon inherent to the NPCC, responsible for unbalancing of the neutral point [55][56], potentially resulting in distorted output waveforms. The mechanisms were discussed in Chapter 4. Severe unbalance can cause the capacitor voltages to drift, potentially leading to diode and switch destruction. As can be seen in the measured results, this was not the case for the NPCC being tested. The 3 kHz harmonic components are relatively small, peaking at approximately 630 mA. The individual DC bus voltages measured showed no sign of neutral point variation. This is largely due to the large DC bus capacitor ratings, both C_P and C_N being 5.28 mH.

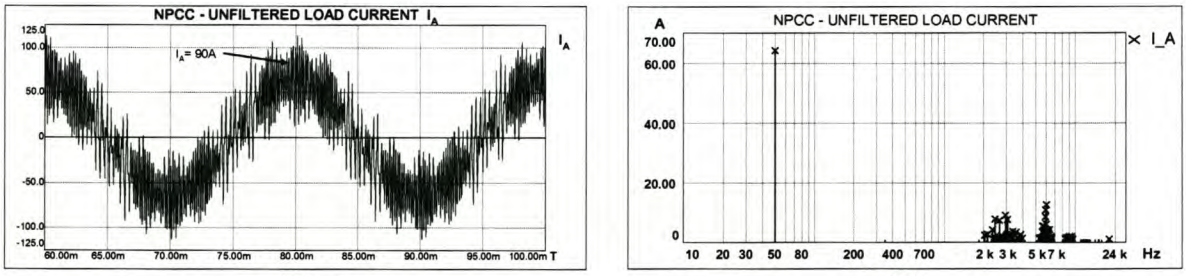


Figure 6-37: Simulated Unfiltered Load Current for the NPCC and FFT Components

Close examination of the ripple current, Figure 6-36(A), shows slight deformation in the rising edge of the fundamental. This is a side effect of using open-loop switching on the NPCC, formed by residual current in the filter inductors, but is remedied when using closed-loop current control [74]. Simulation results of the ripple currents are seen in Figure 6-37. The waveforms are slightly larger in magnitude due to the use of ideal components. Nevertheless, the waveforms are similar to those measured practically, and the presences of the troublesome 3 kHz harmonic components are present, as seen in Figure 6-37(B).

A summary of the high-frequency ripple current harmonics, measured practically on the NPCC, is recorded in Table 9.

6.5.2.4 Investigation Summary

Table 9: Switching Ripple Current Harmonic Magnitudes for 3 Topologies (Load-Side)

Frequency Component	SSC (normal SVM) I_{RMS} = 45.4 A		SSC (Interleaved SVM) I_{RMS} = 43.8 A		NPCC I_{RMS} = 46.4 A	
3 kHz	N/a		N/a		0.63 A	(-4 dB)
6 kHz	5.01 A	(14 dB)	0.40 A	(-8 dB)	7.94 A	(18dB)
12 kHz	6.31 A	(16 dB)	6.03 A	(15.6 dB)	1.00 A	(0 dB)
18 kHz	1.59 A	(4 dB)	0.16 A	(-16 dB)	0.63 A	(-4 dB)
24 kHz	1.45 A	(3.2 dB)	1.51 A	(3.6 dB)	0.25 A	(-12 dB)
30 kHz	0.63 A	(-4 dB)	N/a		0.15 A	(-16.4 dB)
36 kHz	0.32 A	(-10 dB)	0.25 A	(-12 dB)	0.16 A	(-16 dB)
42 kHz	0.13 A	(-18 dB)	N/a		N/a	
48 kHz	0.17 A	(-15.6 dB)	0.16 A	(-16 dB)	N/a	
54 kHz	0.10 A	(-20 dB)	N/a		N/a	
60 kHz	0.25 A	(-12 dB)	0.25 A	(-12 dB)	N/a	
66 kHz	0.16 A	(-16 dB)	N/a		N/a	
72 kHz	0.10 A	(-20 dB)	0.12 A	(-18 dB)	N/a	

The ripple current FFT measurements recorded for both the SSC and NPCC using the different switching techniques are tabulated in Table 9. Using interleaved SVM for the SSC drastically reduces the ripple components at multiples of the 6 kHz switching frequency. The 12 kHz components of the SSC, and multiples thereof, become the dominant switching harmonics. For the NPCC, the 6 kHz ripple components are the only components to exceed any of the SSC ripple components. The NPCC also generates a lower range of switching harmonics. However, the measurements on the transformer secondary, specifically for the SSC, do not necessarily reflect the conditions occurring on the primary of the transformer. Both converters, making up the SSC, expose their primary-side components to the same current ripple components. Thus the benefit of interleaved SVM is only seen on the transformer secondary.

On the SSC using normal SVM, the output ripple current waveform is typical of the switching technique, as discussed. Furthermore, it was observed that the interleaved switching for the three-phase SSC experiences three distinct phase shifts, the result being the large reduction in the ripple current. For the NPCC, the unbalancing 3 kHz components are evident in the measurements; however, due to the switch sequence selection, loading and large DC bus capacitance, stable operation was obtained.

6.5.3 Filtered Load Current and Voltage Waveforms

6.5.3.1 Investigation Criterion

In this section the load currents are measured after filtering to determine quality of the fundamental component each of the topologies is capable of modulating. High and low-frequency analyses of the current and voltage waveforms are performed to determine whether there are typical harmonics prevalent in each of the topologies. The use of open-loop control

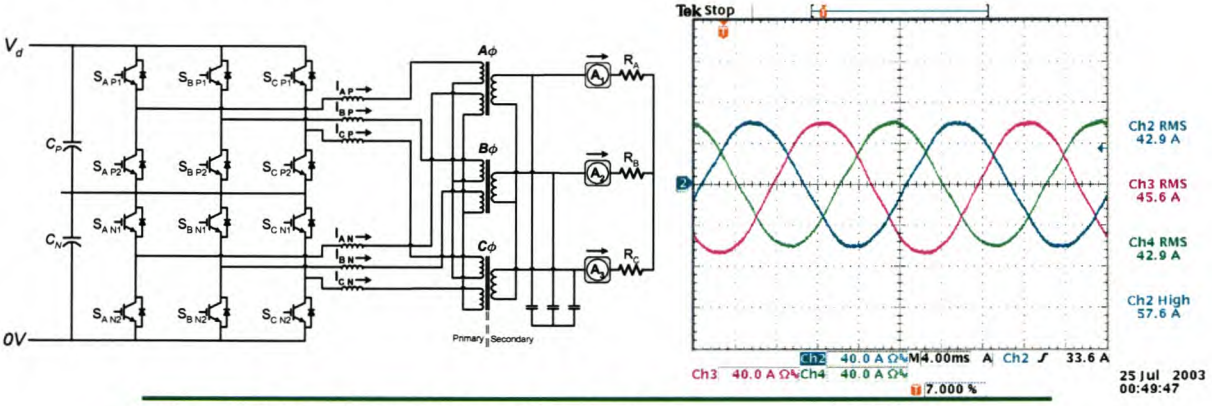
also ensures that harmonics, typical to the NPCC and SSC, are not suppressed.

With the low-pass filters for either topologies having cut-off frequencies of approximately 3.2 kHz, frequencies with lower harmonic numbers can be accurately measured, without the switching harmonics interfering with the measurements. Finally, the load voltages are compared to voltages obtained where the transformer is removed from the circuit, in order to determine the impact, if any, on either topology's waveform modulation. The SSC is compared to a three-phase converter using normal SVM.

6.5.3.2 SSC Measurements Using Normal SVM

6.5.3.2.1 Current Waveforms

The measured three-phase filtered output current waveforms and the measurement points are seen in Figure 6-38.



Measuring Point	Measured Value	Channel on Scope	Description
A_1	I_A	Ch 2	Aϕ Load Current (Transformer Sec.)
A_2	I_B	Ch 3	Bϕ Load Current (Transformer Sec.)
A_3	I_C	Ch 4	Cϕ Load Current (Transformer Sec.)

Figure 6-38: SSC Load Current Measurements – After Filter Capacitors (Normal SVM)

Values recorded, while switching with a m_a of 0.8 and a DC bus voltage of 800 V, range between 42.9 A_{RMS} and 45.6 A_{RMS}.

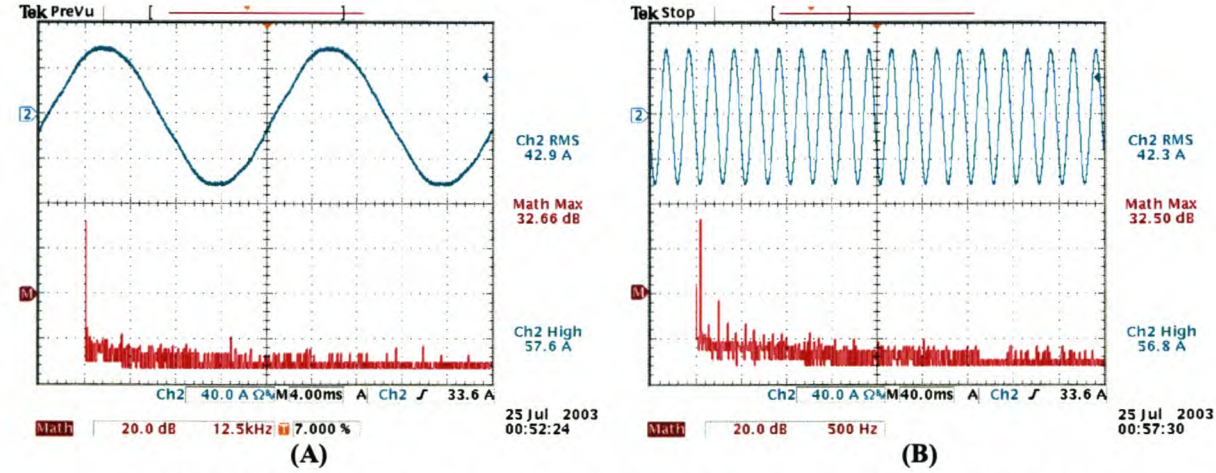
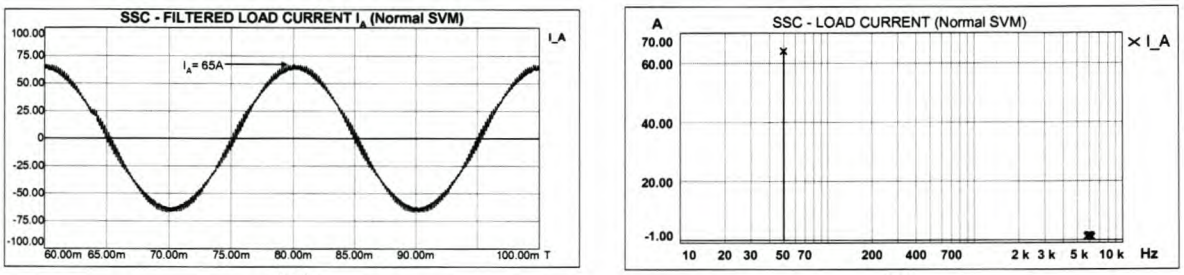


Figure 6-39: A-Phase SSC Load Current Frequency Components (Normal SVM)

The unbalance is a result of load resistance not being totally balanced. FFTs of the A-phase are recorded in Figure 6-38.

In Figure 6-39(A), the effectiveness of the low-pass filter can clearly be seen by the absence of any high-frequency current components, FFT measurement being recorded at 12.5 kHz/div. Figure 6-39(B) records the harmonic components for all values less than the 3.175 kHz cut-off frequency. The DC component measured is not system related, but due to channel offsets on the measurement equipment. A summary of the current harmonic magnitudes can be seen in Table 10, where the Total Harmonic Distortion (THD) is calculated to be 2.16%.

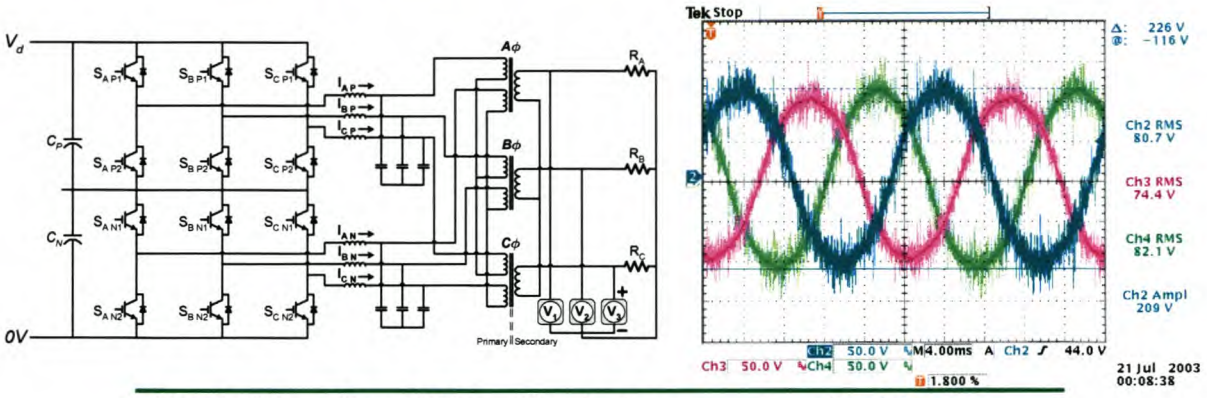


(A) (B)

Figure 6-40: Simulated Load Current and FFT Components for the SSC (Normal SVM)

Simulation results, Figure 6-40, yield waveforms, similar in magnitude, without the effects of the harmonic components on the waveforms. It is thus feasible to use these models for insight into the expected results. The FFT of the simulation shows the presence of a 6 kHz component, not visible in Figure 6-39. This component is visible in Figure 6-40(A), where there is evidence of switching ripple on the fundamental waveform. In practise the system losses damp this component, allowing the filter to completely remove the switching ripple.

6.5.3.2.2 Voltage Waveforms



Measuring Point	Measured Value	Channel on Scope	Description
V_1	V_{A-N}	Ch 2	Aφ Output Voltage (Phase to Neutral)
V_2	V_{B-N}	Ch 3	Bφ Output Voltage (Phase to Neutral)
V_3	V_{C-N}	Ch 4	Cφ Output Voltage (Phase to Neutral)

Figure 6-41: SSC Output Load Voltage Measurements (Normal SVM)

The measured voltages over the load resistors and their measurement points are recorded in

Figure 6-41. The waveforms, like in the case of the SSC using normal SVM, are unbalanced, due to the unequal load resistors. The high-frequency components are a result of measurement noise.

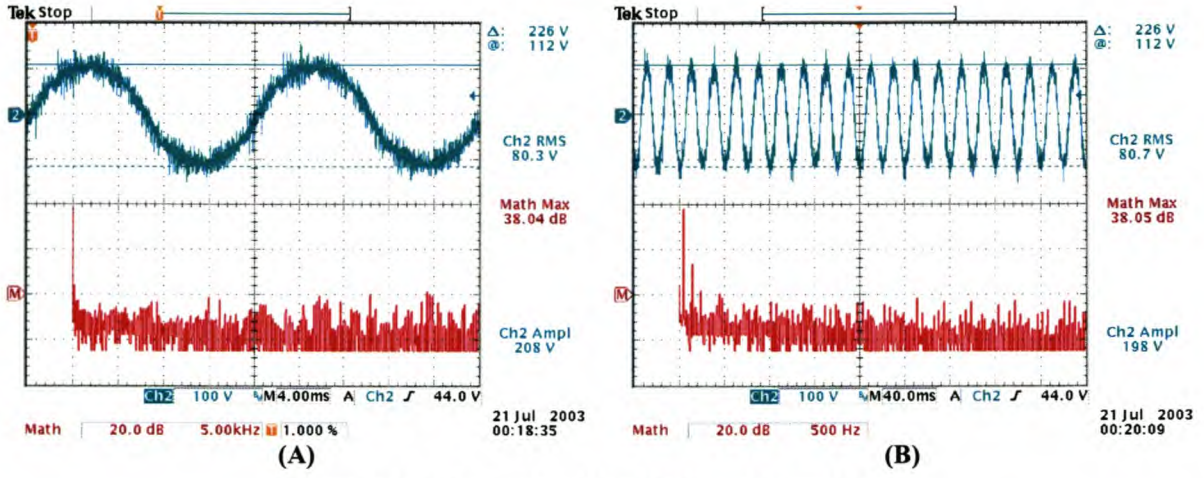


Figure 6-42: SSC A-Phase Load Voltage (Normal SVM)

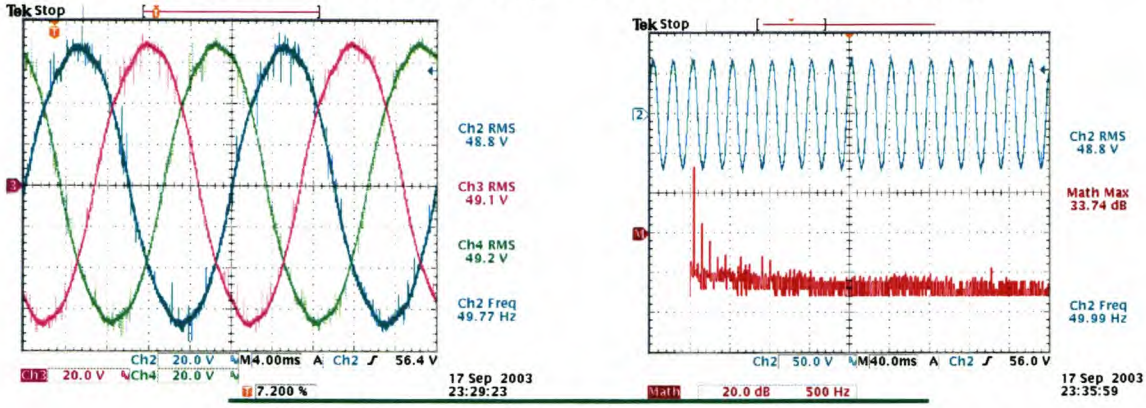
The voltage waveforms offer further insight into the quality of the waveforms. The first observation is the absence any switching harmonic in the voltage, observed in Figure 6-42(A), the measurement taken at 12,5 kHz/div. Any 6 kHz components in the current waveforms would become even more evident in the voltage waveforms. In Figure 6-42(B) a 3rd harmonic voltage component measuring 5 V (14dB) is observed, far larger than the 5th harmonic observed. This is exactly the opposite of the current measurements in Figure 6-38. Its presence, however, is normal and expected. The transformer, made up of six individual single-phase transformers, causes it. Third harmonic currents occur at three times the fundamental frequency in all three phases. This means that they are 360° out of phase with each other, i.e. in phase with each other. Flowing in each phase to a star point, the currents cannot sum to zero, like the 50 Hz fundamental, and hence require a neutral connection back to their source to flow. 3rd harmonic voltages can, however, exist in each phase in a three-wire system, between the phased and neutral or ground, and result in the neutral potential not being zero. The neutral oscillates around the zero point at three times the fundamental frequency. If a neutral is connected, the 3rd harmonic currents are permitted to flow and the 3rd voltage harmonic is suppressed [60].

For this comparison the SSC requires that all the windings on the primary side be totally isolated, creating the three-winding transformer. The topology also requires that none of the windings be earthed. Earthing would prevent the SVM from operating correctly, as the zero states are lost. On the secondary, the load is made up of three resistors in a three-wire configuration. This was done to ensure that the full ratings of the transformer could be utilised, as it is the device that limits the power levels of the topologies.

The isolated neutrals on either side prevent 3rd harmonic current flow resulting in the magnetic fluxes inducing a voltage in the three-wire system. The transformer thus experiences

increased voltage stress. A 5 V 3rd harmonic component was measured in the experiment. The limited 3rd harmonic current components, Figure 6-39, are attributed to capacitive coupling between the neutral point of the load and the transformer, as well as the filter capacitors and the transformer, creating a path, albeit a high impedance, back to the source [60]. It should be noted that the condition discussed only occurs for the 3rd harmonic components

When comparing the voltage waveforms to results obtained from a full-bridge three-phase converter unit, Figure 6-43, the presence of the 3rd harmonic voltages is again observed. However, the unit, a single module of the SSC, was switched directly into a balanced resistive load excluding the transformer. This leads to the conclusion that the 3rd harmonic components are not exclusively a result of load imbalances and failure to connect the transformer neutral. The open-loop modulation strategy also contributes to the distortion.



Measured Value	Channel on Scope	Description
I_A (ϕ-N)	Ch 2	Aϕ Load Voltage
I_B (ϕ-N)	Ch 3	Bϕ Load Voltage
I_C (ϕ-N)	Ch4	Cϕ Load Voltage

Figure 6-43: Single 3-Phase Converter Unit Output Voltage (Balanced Load)

The 3rd, 5th, 7th, 9th and 11th harmonic voltage components are present in Figure 6-43(B), the THD measured being 5.36%. With no control available for compensating for the waveform deformation, this is to be expected. Closed-loop control would allow compensation for these components.

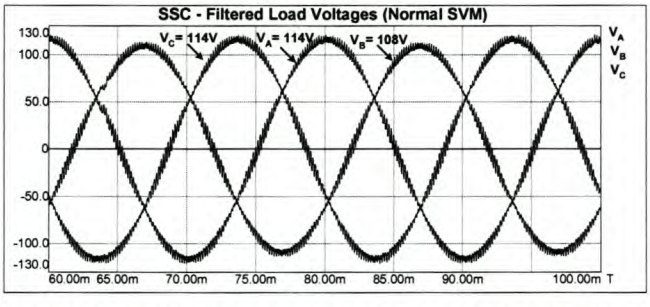
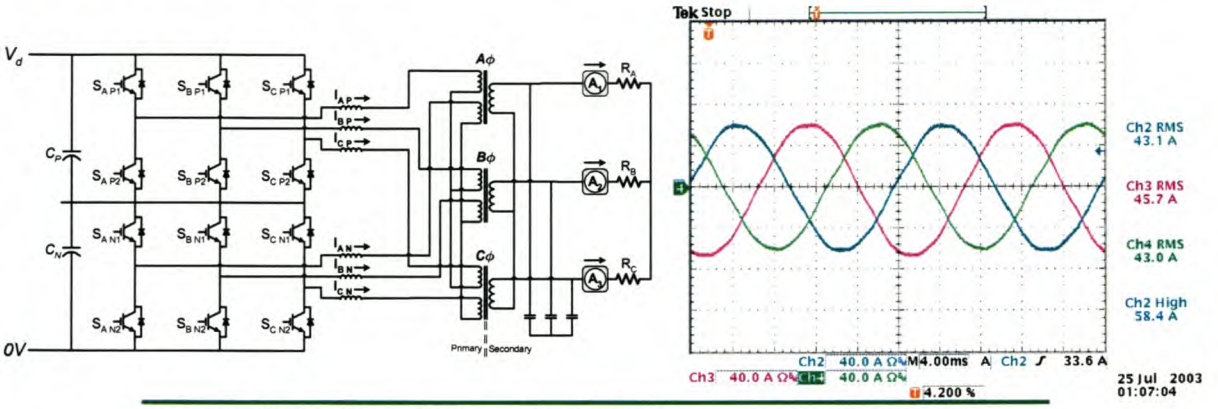


Figure 6-44: Simulated Load Voltage for the SSC (Normal SVM)

The simulated load voltages, Figure 6-44, have peak magnitudes comparable to those measured on the practical converter. Also more evident than in the current waveform simulations is the switching ripple component.

6.5.3.3 SSC Measurements Using Interleaved SVM

6.5.3.3.1 Current Waveforms



Measuring Point	Measured Value	Channel on Scope	Description
A_1	I_A	Ch 2	Aϕ Load Current (Transformer Sec.)
A_2	I_B	Ch 3	Bϕ Load Current (Transformer Sec.)
A_3	I_C	Ch 4	Cϕ Load Current (Transformer Sec.)

Figure 6-45: SSC Filtered Load Currents (Interleaved SVM)

In Figure 6-45, the load currents of the SSC using interleaved switching are recorded. The absence of any high-frequency components is confirmed in Figure 6-46(A). The low-frequency components, Figure 6-46(B), are similar to those recorded for the SSC using normal SVM.

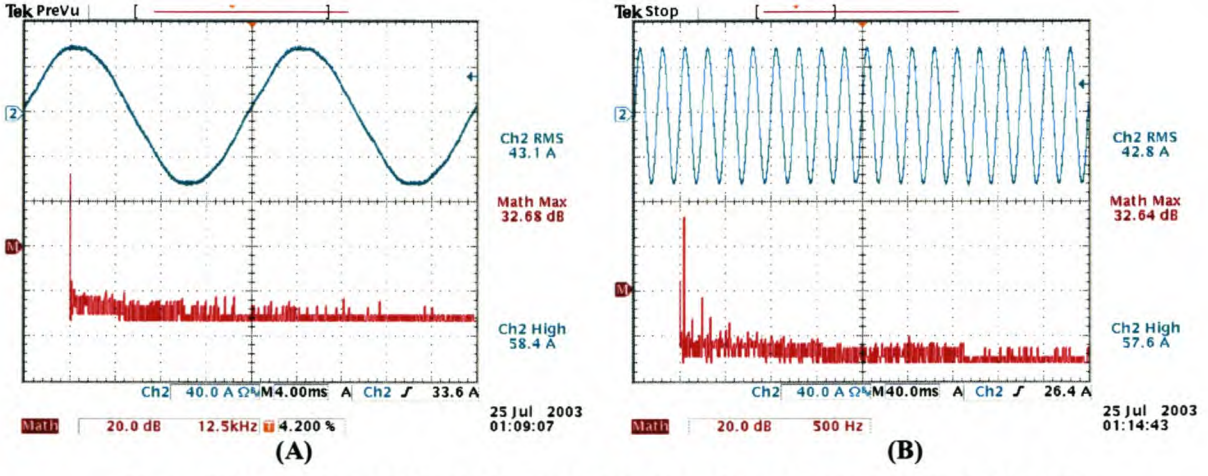
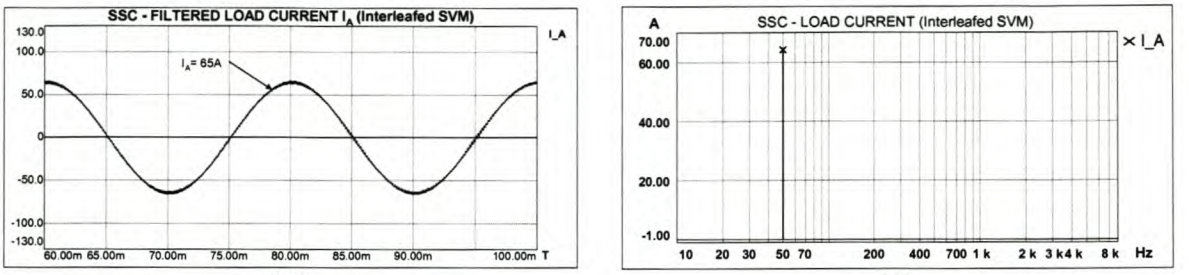


Figure 6-46: A-Phase SSC Load Current Frequency Components (Interleaved SVM)

The FFT measurement values are recorded in Table 10, and the calculated THD for the load current is 1.96%, an improvement on the SSC using normal SVM. Although little visual improvement in the load current quality is seen, the THD proves differently.

Further benefit is seen in SSCs employing numerous levels. With enough levels, and obtaining results superior to those in Figure 6-31, filter capacitors need not be used. This is a considerable component saving that occurs if the filter capacitors need to be located on the converter side of the transformer. Figure 6-47, the simulated results, does not show any evidence of the 3rd, 5th and 7th harmonic components measured in Figure 6-46. This is because

the circuit used ideal components, so switching effects and load anomalies do not influence the result.

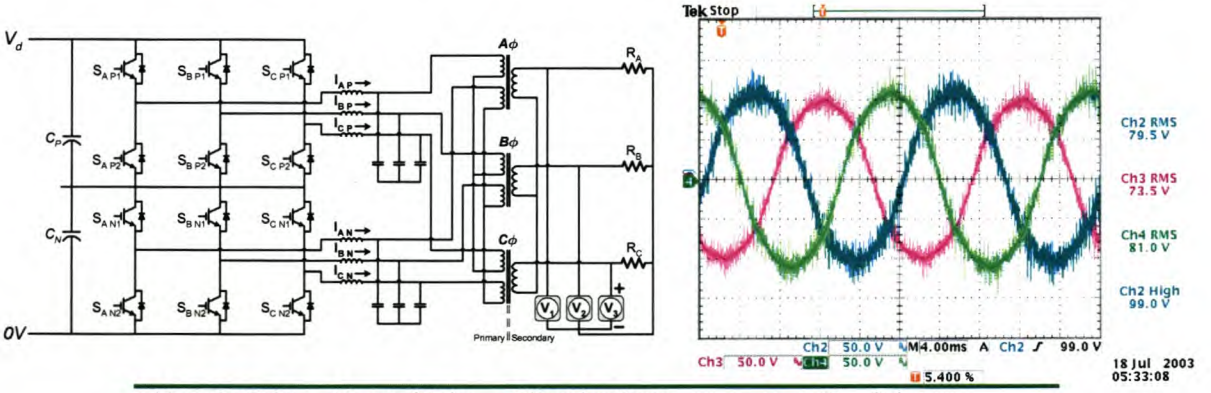


(A) (B)

Figure 6-47: Simulated Load Current FFT Components for the SSC (Interleaved SVM)

The 6 kHz component in the FFT is also absent, an expected result. There is also very little evidence of switching harmonics on the fundamental Figure 6-47(B). Interleafing, as discussed in Chapter 4, pushes the dominant switching frequency to 12 kHz. This result was practically verified.

6.5.3.3.2 Voltage Waveforms



Measuring Point	Measured Value	Channel on Scope	Description
V_1	V_{A-N}	Ch 2	Aϕ Output Voltage (Phase to Neutral)
V_2	V_{B-N}	Ch 3	Bϕ Output Voltage (Phase to Neutral)
V_3	V_{C-N}	Ch 4	Cϕ Output Voltage (Phase to Neutral)

Figure 6-48: SSC Output Load Voltage Measurements (Interleaved SVM)

In Figure 6-48 the measured output voltage waveforms using interleaved switching are displayed. The waveforms, unbalanced due to the load, also appear to posses less measurement noise. This is also evident in Figure 6-49(B), when comparing it to the SSC scheme using normal SVM. This is attributed to the interaction of the higher apparent switching frequency to surrounding noise.

The effect of load imbalance and the transformer connection is also observed in the harmonic analysis, Figure 6-49(B), where the 3rd harmonic is larger than the 5th, opposite to what is seen in the harmonic current analysis. The simulated load voltages of the interleaved SSC, Figure 6-50, yield waveforms with hardly any distortion or switching ripple.

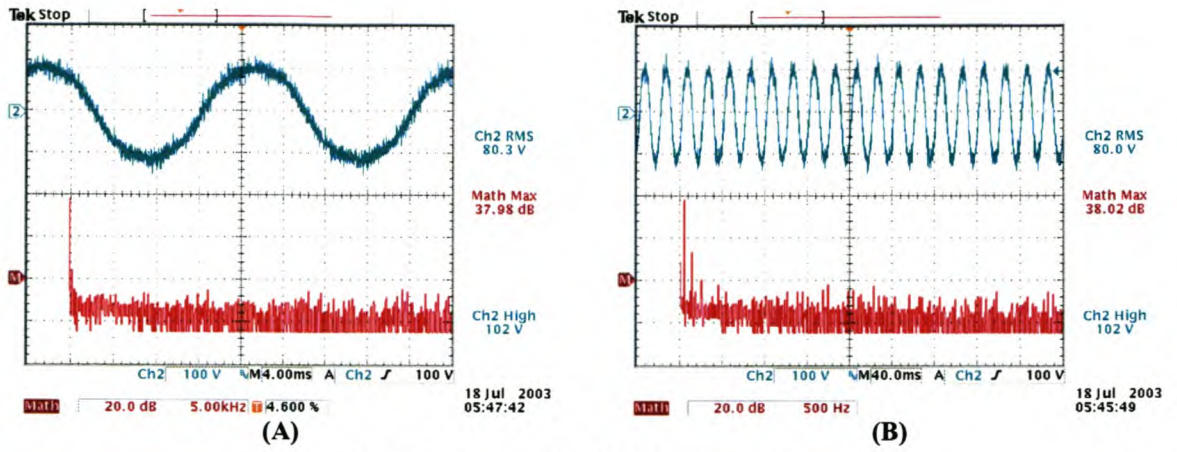


Figure 6-49: SSC A-Phase Load Voltage (Interleaved SVM)

The magnitudes of the peak values are also comparable to those measured on the practical converter.

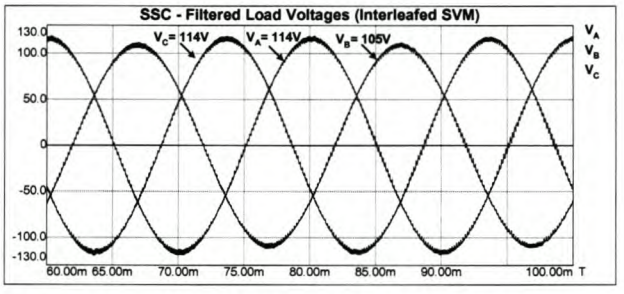
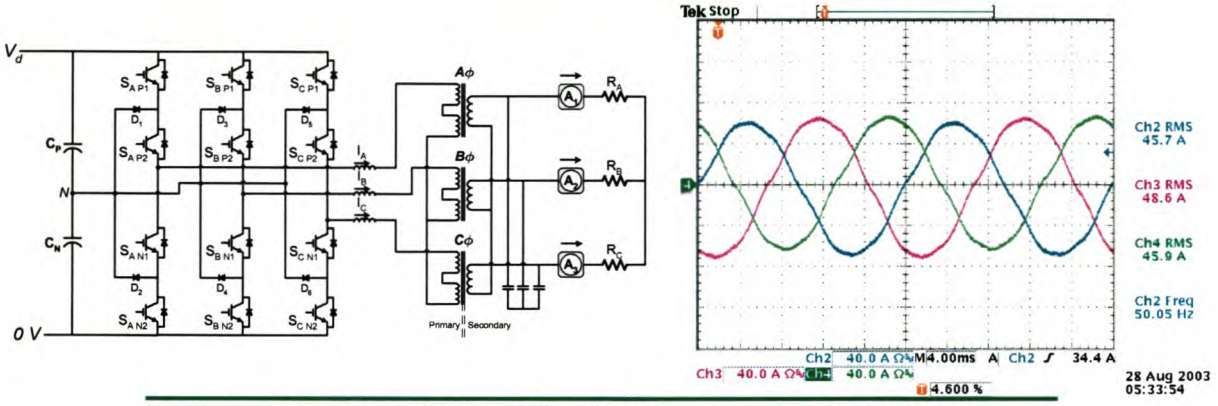


Figure 6-50: Simulated Load Voltage for the SSC (Interleaved SVM)

6.5.3.4 NPCC Measurements Using 3-Level SVM

6.5.3.4.1 Current Waveforms



Measuring Point	Measured Value	Channel on Scope	Description
A_1	I_A	Ch 2	Aϕ Load Current (Transformer Sec.)
A_2	I_B	Ch 3	Bϕ Load Current (Transformer Sec.)
A_3	I_C	Ch 4	Cϕ Load Current (Transformer Sec.)

Figure 6-51: NPCC Filtered Load Currents

Finally, the load currents for the NPCC, after filtering, are measured and displayed in Figure 6-51. Most noticeable on the waveforms is the distortion compared to that measured

on the SSC. An explanation for the waveform distortion is obtained by considering the FFT measurements of the load current, seen in Figure 6-52. In Figure 6-52(A), small 5, 6, 10 and 15 kHz components are measured. They are attributed to measurement noise. The 5, 10 and 15 kHz components are attributed to noise. However, the 6 kHz components can be seen on the current waveform, indicating that the low-pass filter circuit has not removed the switching ripple completely. The cut-off frequency of the filter used was 3.2 kHz.

In Figure 6-52(B), the frequency harmonics at the lower end of the spectrum are recorded. The 3rd, 5th, 7th and 9th harmonic components are slightly larger than those recorded on the SSC, using both switching techniques, with the values recorded tabulated in Table 10. The appearance of 100, 200 and 300 Hz components requires extra explanation.

The 100 Hz components are clearly visible on the measured current waveform in Figure 6-51 and Figure 6-52, and are attributed to the waveform distortion discussed in the section on the unfiltered load current. The per-phase 3-level output combined with the freewheeling paths and counter Emf cause this distortion. With no negative voltage applied to the inductor from the converter side, the current decay time during freewheeling is longer than that experienced in the SSC. This condition poses few problems for the greater of the fundamental period. However, during the zero crossing time, the problem is escalated, resulting in deformation of the rising flank of the fundamental component.

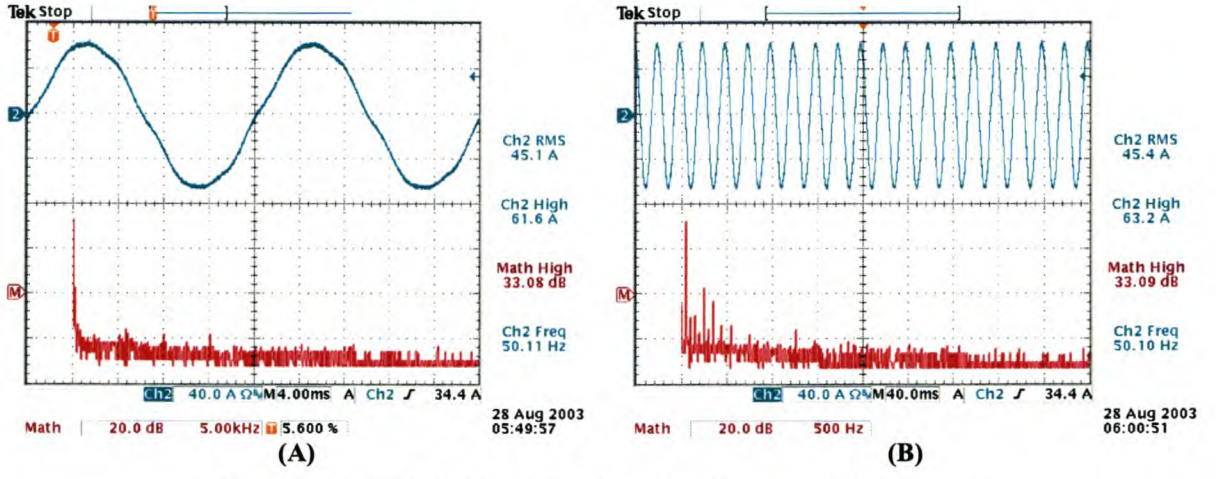
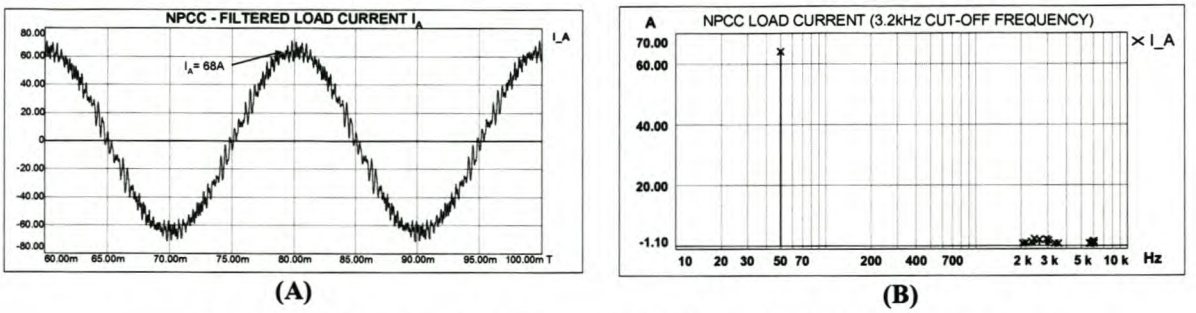


Figure 6-52: A-Phase NPCC Load Current Frequency Components

As this occurs on each of the three phases, twice every fundamental period, the 100 and 200 Hz components become more prominent. It must also be said that these components are considerably reduced when employing closed-loop control. The 300 Hz components are attributed to sector changeovers in the 3-level SVM technique, where more than one switch is operated within a switching state change. Summing the even and odd current harmonics yields a THD of 3.62% for the NPCC.

The simulated current waveforms in Figure 6-53, like those of the SSC models, show no indication of the lower frequency harmonics, but do show the presence of the 3 kHz component discussed in Chapter 4, arising from the switching technique. As the cut-off frequency is

approximately 3.2 kHz, their presence is expected. On the practical converter they were, however, not measured.

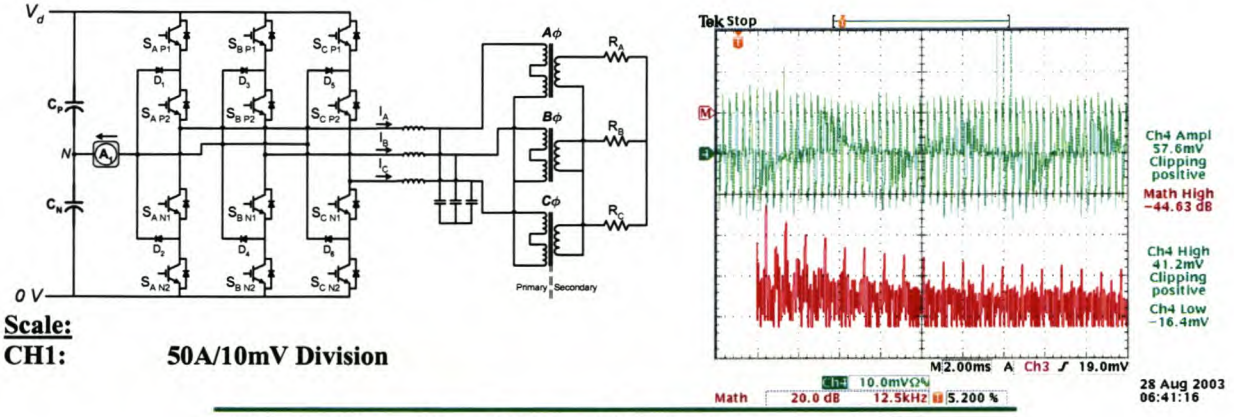


(A) (B)

Figure 6-53: Simulated Load Current FFT Components for the NPCC

The reason for this is the low-pass characteristic of the transformer not allowing the 3 kHz harmonic components to propagate through to the load. The simulated result also indicates a 6 kHz component in the current waveform. This, as was the case for the SSC, is attributed to the simulation not experiencing the same system losses and damping as experienced by the practical device.

6.5.3.4.2 Neutral Point Currents



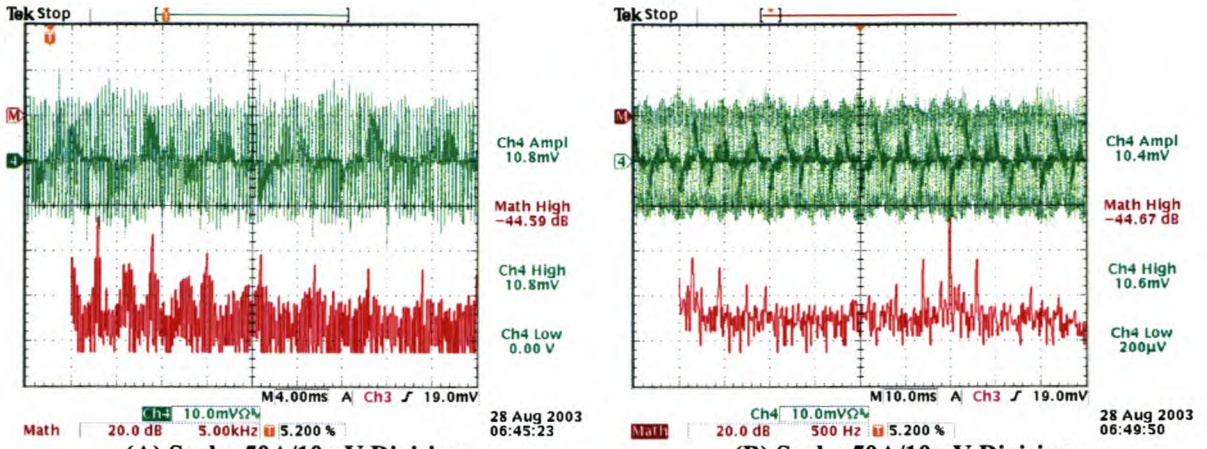
Scale:
CH1: 50A/10mV Division

Measuring Point	Measured Value	Channel on Scope	Description
A_1	I_{NP}	Ch 1	Neutral Point Current

Figure 6-54: NPCC Neutral Point Current Measurement

The 3 kHz components responsible for causing DC bus unbalances are recorded in Figure 6-54 and Figure 6-55, while simulation measurements can be seen in Figure 6-56. The practical measurements indicate a 29 A component occurring at 3 kHz flowing in the neutral point. The simulated result shows a 15 A component occurring at 3 kHz. While the values are different, their incidence, and that of the multiples of the 3 kHz components, is identical.

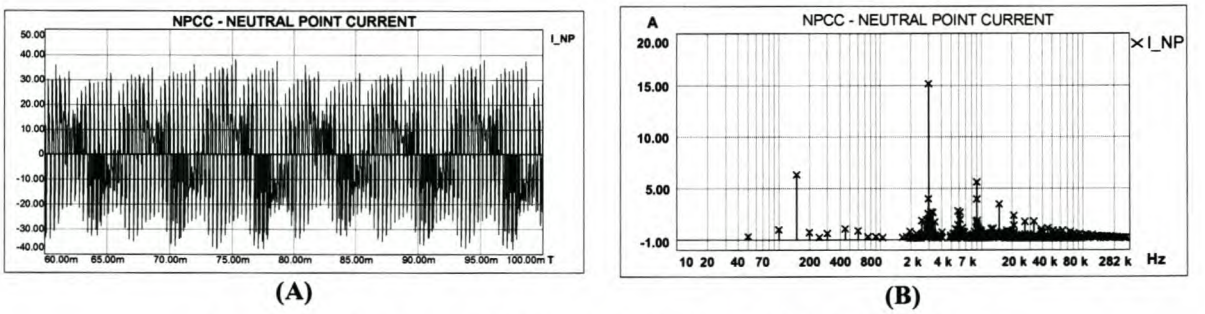
The difference in current magnitudes can partly be attributed to the simulation model seeing a higher 3 kHz impedance than those in the practical NPCC. Re-evaluating Figure 6-52(A&B), it is seen that in the practical NPCC, no 3 kHz component is measured in the load current, while it is present in the simulation model.



(A) Scale: 50A/10mV Division **(B) Scale: 50A/10mV Division**

Figure 6-55: NPCC Neutral Point Current Harmonic Components

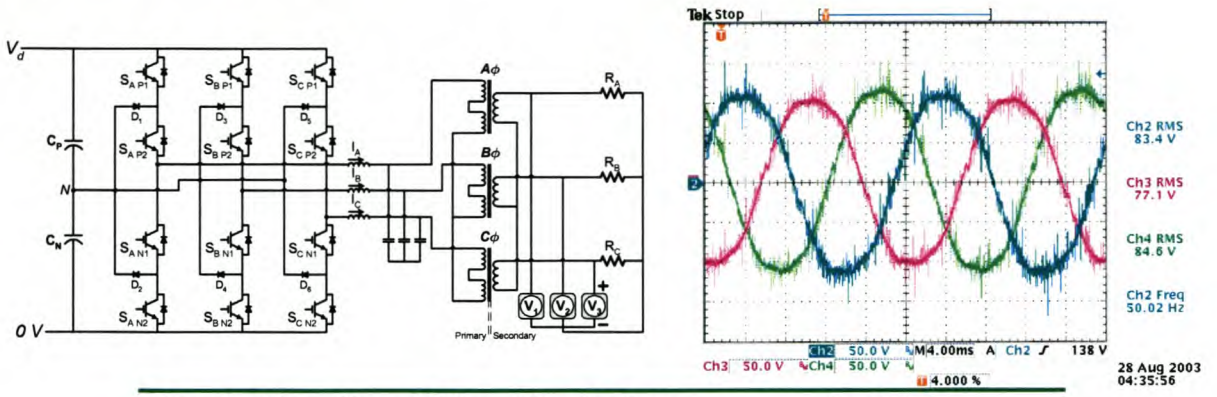
This implies that the filter capacitors in the practical device have lower 3 kHz impedances than that in the simulation, hence the higher current magnitudes in the practical measurements.



(A) **(B)**

Figure 6-56: Simulated Load Current FFT Components for the NPCC

6.5.3.4.3 Load Voltages



Measuring Point	Measured Value	Channel on Scope	Description
V_1	V_{A-N}	Ch 2	Aϕ Output Voltage (Phase to Neutral)
V_2	V_{B-N}	Ch 3	Bϕ Output Voltage (Phase to Neutral)
V_3	V_{C-N}	Ch 4	Cϕ Output Voltage (Phase to Neutral)

Figure 6-57: NPCC Output Load Voltage Measurements

The load voltage measurements, Figure 6-57, and the FFTs of the measured A-phase voltage, Figure 6-58, indicate similar results to those measured in the current waveforms. One

exception is that the switching frequency harmonic component is far more prominent in the voltage waveforms than in the current waveforms. In contrast to the SSC, FFTs of the voltage waveform of NPCC imply that the NPCC contributes less to surrounding noise. This is evident when comparing Figure 6-58(A) to Figure 6-42(A) and Figure 6-49(A).

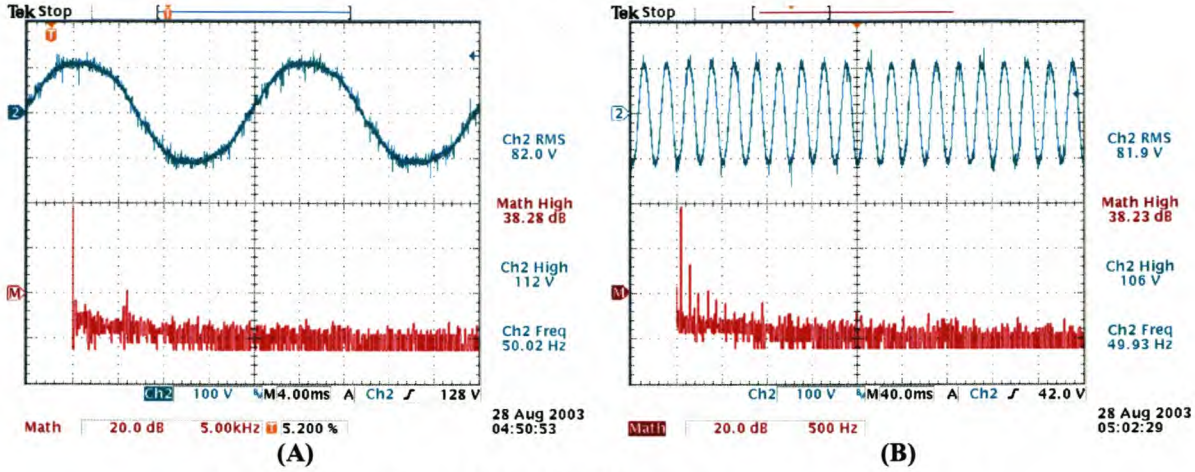
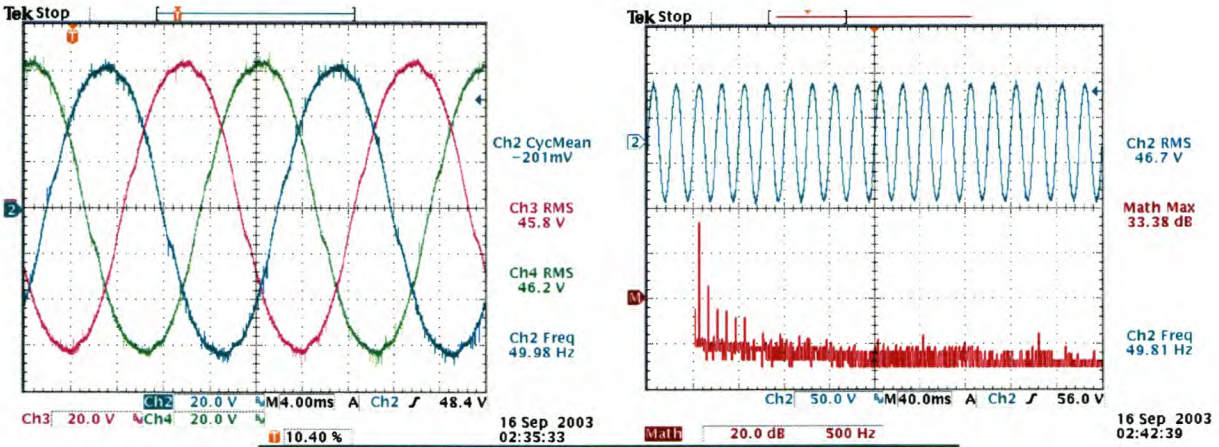


Figure 6-58: A-Phase NPCC Load Voltage Frequency Components

A comparison is also made between the output voltages of the NPCC switching through the transformer and an NPCC switching directly into the balanced three-phase resistive load, recorded in Figure 6-59. The comparison again confirms that the presence of the lower frequency harmonic components is a by-product of the modulation strategy and the isolation transformer. With the open-loop modulation, interaction between the three-wire load, results in deformation of the modulated waveform. The calculated THD of the measured waveforms in Figure 6-59 is 4.58%.

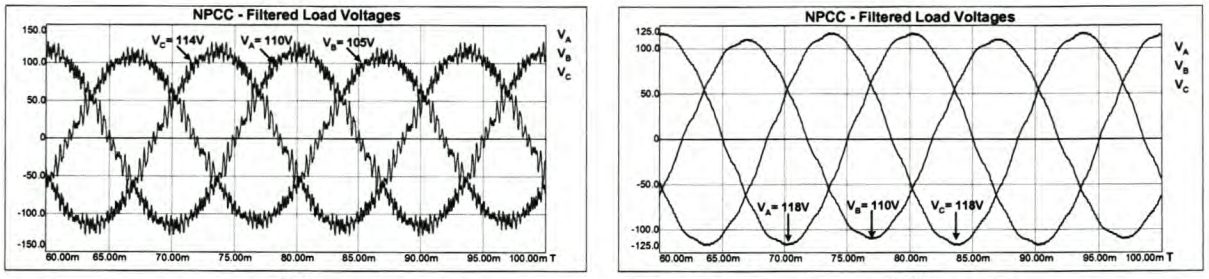


Measured Value	Channel on Scope	Description
I_A (ϕ-N)	Ch 2	Aϕ Load Voltage
I_B (ϕ-N)	Ch 3	Bϕ Load Voltage
I_C (ϕ-N)	Ch4	Cϕ Load Voltage

Figure 6-59: NPCC Converter Unit Output Voltage (Balanced Load and No Transformer)

The simulated voltages, Figure 6-60(A), indicate that for a cut-off frequency of 3.2 kHz, the load voltage waveform contains large 3 kHz components. Figure 6-60(B), a simulation model with a filter cut-off frequency of 1 kHz, shows similar distortions to those seen in the

current waveforms. Also evident in Figure 6-60(B) is a 600 Hz distortion occurring on the waveform. Mentioned when considering the load current waveform distortion, it is a result of sector changeover while using 3-level SVM (5.3.2).



(A) (B)

Figure 6-60: Simulated NPCC Load Voltages (A) 3.2 kHz Cut-Off Frequency (B) 1 kHz Cut-Off Frequency

A sector changeover, occurring every 60° in the control strategy, results in two of the phase-arms changing state, increasing the switching harmonic in this area. While using open-loop modulation, this phenomenon cannot be mitigated. Closed-loop control enables the waveform distortion to be compensated for.

6.5.3.5 Investigation Summary

By investigation of the filtered output quantities of the three switching schemes, further information regarding the two topologies has been identified.

For the SSC topologies required to operate using an isolation transformer, grounding or connection of the secondary winding is necessary to prevent 3rd harmonic voltages being generated on the load side. The three-winding transformer would have to be overrated in order for the transformer to source the 3rd harmonic currents that could potentially exist.

For the NPCC, the low-pass filters are required to have cut-off frequencies well below half the switching frequency. Open-loop modulation also shows that the waveforms of the NPCC contain a larger quantity of low-frequency harmonics generated by the numerous switching states available. The choice of switching sequences in 3-level SVM also has a large impact on the quality of the modulated output waveform. Table 10 summarises the performances of each of the topologies using their respective switching techniques. The THD and efficiency values were calculated using MATLAB®, the routines documented in Appendix E.

It can be seen that the SSC using normal and interleaved SVM produces the best quality modulated current waveforms while using open control, while the NPCC has the largest current waveform THD. The THD measurements of the voltage waveforms contradict the current results. This leads to the conclusion that the SSC voltage waveforms are more susceptible to 3rd harmonic voltages, generated by the transformer connection.

The voltage waveform comparisons, between Figure 6-42 and Figure 6-43 and again between Figure 6-58 and Figure 6-59, show that the harmonics are caused by the modulation strategies and the transformer connections. The measured THD for the SSC in Figure 6-43 was 5.36%, while the NPCC in Figure 6-59 yielded a THD of 4.58%. Considering that only

one converter unit was used to measure the SSC modulation capability, the benefit of interleaved SVM was not obtained. Furthermore, it can be concluded that using closed-loop control would mitigate the converter-generated harmonics.

Table 10: Load Current Harmonic Magnitudes for 3 Topologies (Load-Side)

Frequency Component	SSC (normal SVM) I_{RMS} = 42.9 A		SSC (Interleaved SVM) I_{RMS} = 42.8 A		NPCC I_{RMS} = 45.4 A	
50 Hz (Fund.)	42.17 A	(32.5 dB)	42.85 A	(32.64 dB)	45.13 A	(33.09 dB)
100 Hz (2nd)	N/a		N/a		0.28 A	(-11 dB)
150 Hz (3rd)	0.23 A	(-12.8 dB)	0.25 A	(-12 dB)	0.35 A	(-9 dB)
200 Hz (4th)	0.0 A		0.0 A		0.14 A	(-17 dB)
250 Hz (5th)	0.76 A	(-2.4 dB)	0.69 A	(-3.2 dB)	1.36 A	(2.7 dB)
300 Hz (6th)	0.0 A		0.0 A		0.16 A	(-16 dB)
350 Hz (7th)	0.23 A	(-12.8 dB)	0.25 A	(-12 dB)	0.67 A	(-3.5 dB)
450 Hz (9th)	0.14 A	(-16.8 dB)	0.13 A	(-18 dB)	0.20 A	(-14 dB)
550 Hz (11th)	0.23 A	(-12.8 dB)	0.20 A	(-14 dB)	0.20 A	(-14 dB)
650 Hz (13th)	0.16 A	(-16 dB)	0.10 A	(-20 dB)	0.0 A	
750 Hz (15th)	0.13 A	(-18 dB)	0.13 A	(-18 dB)	0.13 A	(-18 dB)
850 Hz (17th)	0.13 A	(-18 dB)	0.13 A	(-18 dB)	0.0 A	
950 Hz (19th)	0.13 A	(-18 dB)	0.10 A	(-20 dB)	0.0 A	
1250 Hz (25th)	0.0 A		0.0 A		0.16 A	(-16 dB)
1500 Hz (30th)	0.0 A		0.0 A		0.10 A	(-20 dB)
% THD I	2.93%		2.99%		4.21%	
% THD V (with TRFR)	12.61%		9.95%		7.69%	
% THD V (No TRFR)	5.36%				4.58%	
Efficiencies	81%		80%		90%	

Using data recordings of the measured current and voltage waveforms, accompanied with the measurement of the DC bus quantities supplying the re-configurable converter while switching into the load, the efficiencies for all three switching techniques were obtained and tabulated in Table 10. It was found that the SSC, using either switching technique, has an efficiency of approximately 80%, while the NPCC yields an efficiency of approximately 90%. The higher efficiency of the NPCC is partly due to the reduced power loss in half of the switches making up the topology.

These measured values serve only to supply an indication of the typical efficiencies expected from the topologies. Much can be done to improve the efficiencies of either topology.

6.6 Topological and Switching Technique Assessment on Converter Components

The successful operation of both topologies is not only dependent on the modulation techniques and converter structure, but also the various essential components within the topologies. It is therefore necessary to assess the impact of the topology structure and switching schemes used on these vital components within the converters. Two components are ear-

marked for investigation. The first is the DC bus capacitors and the second is the filter inductors. The objective of this investigation is to aid the decision-making process when considering either of the topologies.

6.6.1 DC Bus Capacitor Currents

6.6.1.1 Investigation Criterion

Capacitor failure has been deemed as the primary source of failure within power electronic converters. According to [58], 60% of failures in switchmode power supplies are caused by the failure of the electrolytic capacitors. Determining the topology impact on them is done by way of practical measurements. These measurements are compared to simulation results. In the topology assessments on the bus capacitors, it is the lower frequency components that are of interest. High-frequency ripple currents through electrolytic capacitors do not affect their lifespan as severely as the lower frequency components [57][58][79][80]. The reason is that as frequency increases, the equivalent series resistance (E.S.R.) of the capacitors drops in a near linear fashion. High-frequency components thus have lower impact on the capacitor life span, one of the reasons why they are used extensively in converter applications.

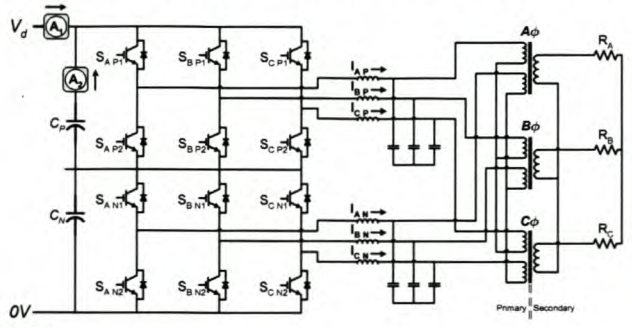
Temperature is the primary concern when considering the impact on capacitor life span. Current flowing through the capacitors (E.S.R.) causes losses in the form of heat and an increase in temperature. The temperature increase causes electrolyte levels, vaporised by the heating, to drop. The safety mechanism, preventing dangerous pressure build-up, permits electrolyte vapour to escape through the capacitor's casing. Lost to the system, a larger area of the capacitor plates, previously covered by the electrolyte, are left exposed. This increases the E.S.R., which in turn increases the heating of the capacitors.

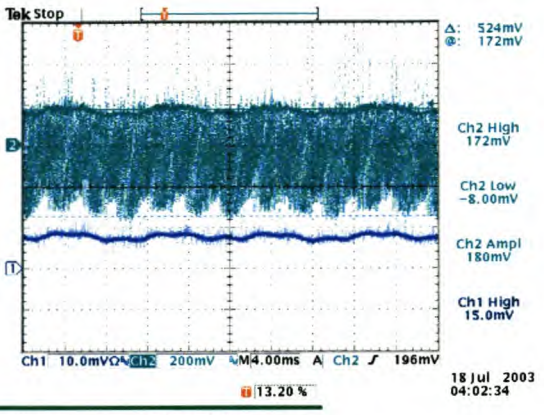
The most telling indication of the impact that the two topologies have on the DC bus capacitors is the power loss within the capacitors. I^2R losses are used in combination with various temperature related conditions to determine the capacitor's expected lifespan. Datasheets also provide de-rating constants for the E.S.R. when exposed to higher frequency current components. For these tests, performed in a near identical temperature environment, external temperature conditions are assumed constant. Determining the power loss due to the ripple currents for both topologies is therefore an accurate indication of the impact that the topologies have. The aim is not to determine the expected life span but the losses.

6.6.1.2 Practical SSC Results Using Normal SVM and Interleaved Switching

For the SSC converter topology both switching techniques, normal and interleaved SVM, impact on the DC bus capacitors in the same way. Both modules effectively operate individually and thus only impact the DC bus capacitors to which they are connected. For this reason it is possible to evaluate the SSC, using either switching scheme, since the effect on the capacitors would be identical. Figure 6-61 is a record of the DC currents measured on the

SSC while operating with an 800 V bus and a m_a of 0.8. The relevant scaling factors of the current waveforms are noted below the figure of the measurement points.



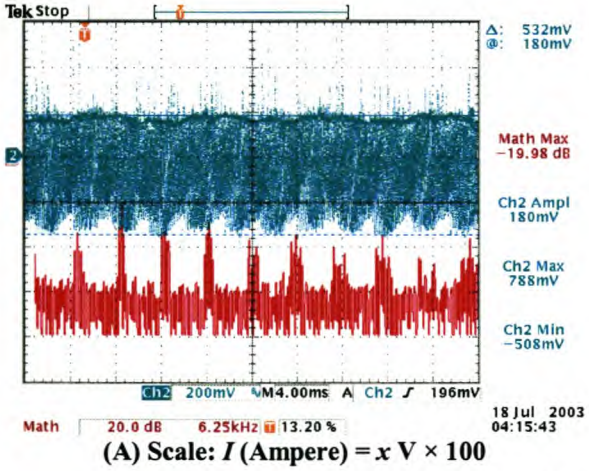


Scale:
Ch1: 20A/10mV Division
Ch2: I (Ampere) = x V × 100

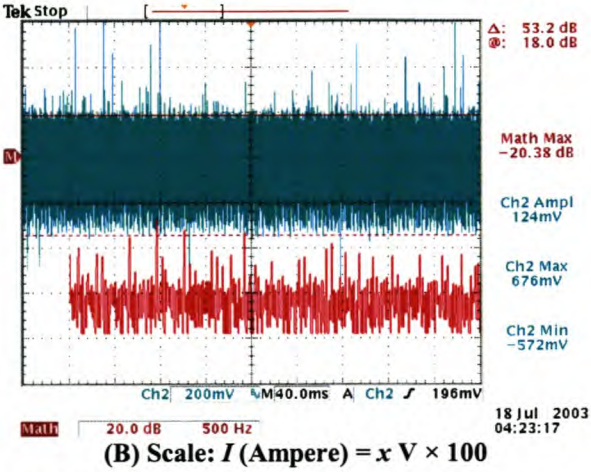
Measuring Point	Measured Value	Channel on Scope	Description
A_1	I_{DC}	Ch 1	DC Source Current
A_2	I_{CP}	Ch 2	Capacitor C_P's Current

Figure 6-61: SSC (Normal SVM) DC Source and Bus Capacitor Current Measurements

In an ideal system, it would not be necessary to measure the DC supply, as it is assumed to contain no ripple current. However, in many practical applications, as was the case for these tests, the DC supply current, 30.4 A in magnitude, has a ripple component caused by the phase imbalance on the three-phase supply. It is necessary to measure the harmonic content to ensure that the SSC topology is not accused of causing the supply side ripple currents. The DC supply ripple contains a 1.25 A 2nd and a 0.8 A 6th harmonic component. This measurement provides a reminder that the supply currents also flow through the DC bus, since one of its functions is to provide isolation between the power network and the converter output. When rating the DC bus capacity, the supply currents, potentially affecting the capacitor life span, need to be considered.



(A) Scale: I (Ampere) = x V × 100



(B) Scale: I (Ampere) = x V × 100

Figure 6-62: Ripple Current flowing through DC Bus Capacitor C_P (SSC Topology)

Further investigation of Figure 6-61 shows that by applying the ratios for both measurements, both Ch1 and Ch2 are scaled to measure at 20 A/div. Also evident in the measured

capacitor ripple current, Ch 2, is the positive DC supply ripple superimposed on its waveform. The magnitudes are approximately equal. The current flowing into the DC capacitors is thus only the current ripple measured below the Ch2 measurement axis with peak measurements of approximately 40 A.

With the DC supply harmonic isolated, the ripple current created by the SSC can be determined in the measurement of the current flowing through the DC bus capacitors of the high, Figure 6-62(A), and low, Figure 6-62(B), frequency components are measured. The switching frequency ripple is clearly visible in the high-frequency FFT of Figure 6-62(A), where the largest component is recorded at 12 kHz. The low-frequency FFT, Figure 6-62(B), indicates that the largest component occurs at approximately 950 Hz. Also measured are the more detrimental low-frequency components. A breakdown of the specific components is listed in Table 11. For an approximate E.S.R. value of 15 mΩ and the necessary E.S.R. de-rating curves, obtained from [80], the measured waveform results in a power loss of 0.348 W is calculated for capacitor C_P, using the MATLAB® routines in Appendix E.

The simulation waveforms, Figure 6-63, show similar measurements. Absent in Figure 6-63(A) is the DC supply superimposed on the waveform. The simulation results also show the peak values at approximately 35 A, slightly lower than the practically measured results.

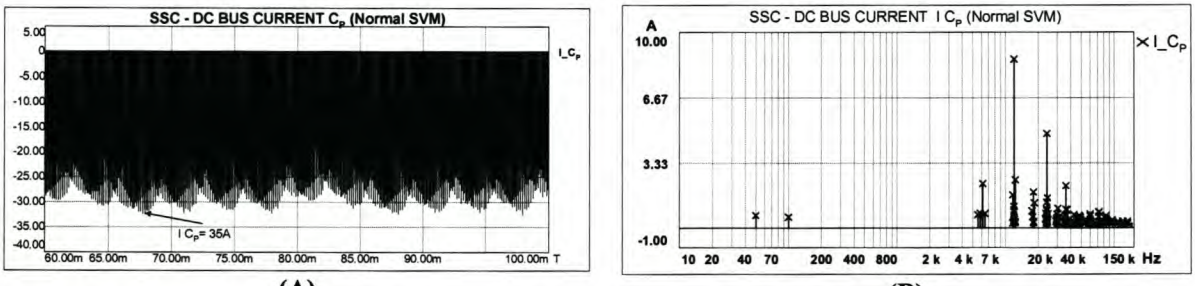


Figure 6-63: Simulated DC Bus Current FFT Components for the SSC

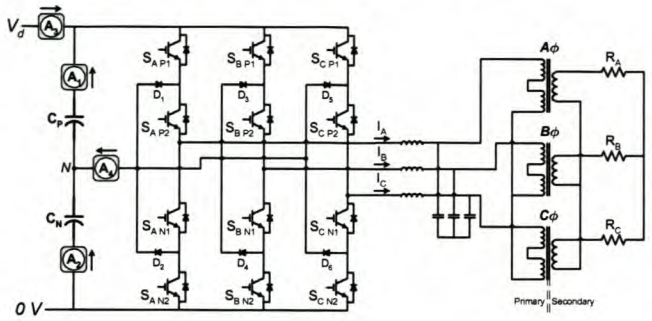
Figure 6-63 (B) shows the FFT breakdown of the various ripple current components. The high-frequency components give evidence to their presence, but the low-frequency components are not observed. Once again this is a result of the component idealities and low simulation system losses.

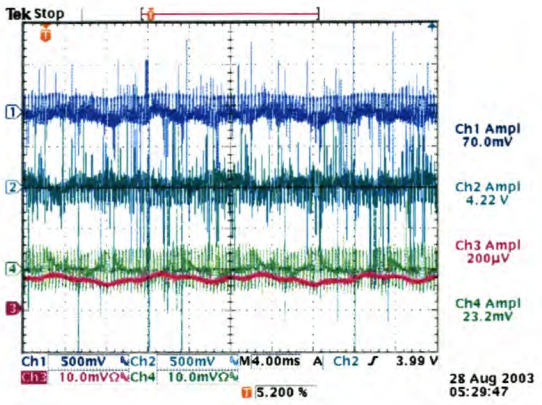
6.6.1.3 Practical NPCC Results Using 3-Level SVM

For the NPCC, identical measurements were recorded. The measurement recorded in Figure 6-64 is of the DC supply current, the neutral point current and both top and bottom capacitor currents, I_{CP} and I_{CN}. The measured DC supply current has a magnitude of 32 A. As was the case for the SSC, harmonics are present in the DC supply. A 1.0 A 2nd harmonic and a 1.0 A 6th harmonic are measured.

For the comparison to the SSC, only the current waveform of Ch1 flowing through capacitor C_P is examined, in order to determine the power dissipated in the capacitor. In Figure

6-65(A&B) the measured high and low-frequency harmonic components are displayed.



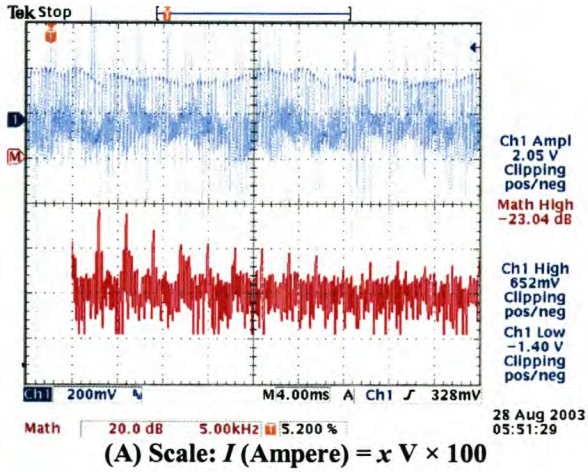


Scale:
Ch1 & Ch2: *I* (Ampere) = *x* V × 100
Ch3: 20A/10mV Division
Ch2: 50A/10mV Division

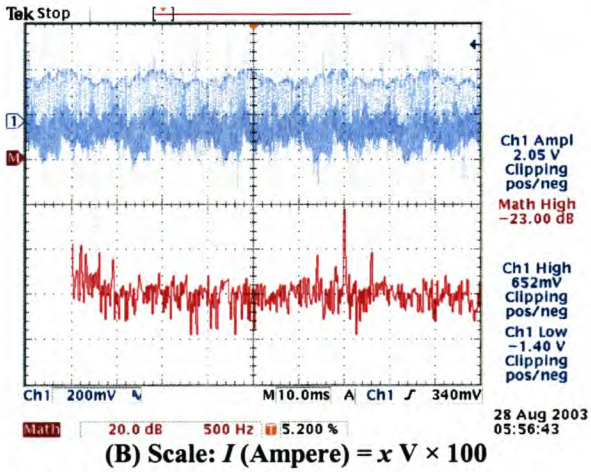
Measuring Point	Measured Value	Channel on Scope	Description
A_1	I_{CP}	Ch 1	Capacitor C_P's Current
A_2	I_{CN}	Ch 2	Capacitor C_N's Current
A_3	I_{DC}	Ch 3	DC Source Current
A_4	I_{NP}	Ch 4	Neutral Point Current

Figure 6-64: NPCC DC Source, Bus Capacitor and Neutral Point Current Measurements

Comparing Figure 6-65(A) to Figure 6-62(A), a large reduction in the switching ripple flowing through the capacitors is seen. Dominant is the presence of the 3 kHz current components in Figure 6-65(B), with a maximum value of 7.1 A. As for the rest of the harmonic spectrum, their values appear small. The dominant harmonic components, less than 1.5 kHz, are recorded in Table 11.



(A) Scale: *I* (Ampere) = *x* V × 100



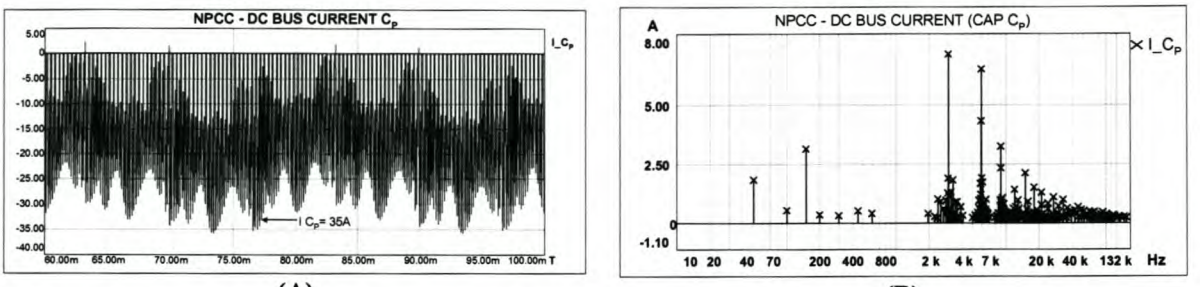
(B) Scale: *I* (Ampere) = *x* V × 100

Figure 6-65: Ripple Current flowing through DC Bus Capacitor C_P (NPCC Topology)

To determine the effects that these components have on the bus capacitor, the same MATLAB® routine used for the SSC was applied to the measured waveform. The calculated power lost in the capacitors, using the same E.S.R. values, resulted in power loss of 0.218 W. This is considerably lower than that measured in the SSC, providing further proof of the NPCC's overall efficiency.

The simulated results, Figure 6-66(A), also show the absence of the DC current superim-

posed on the DC measurement. With peak ripple values of approximately 35 A, it compares slightly higher than that recorded in Figure 6-62(B), approximately 24 A. However, in Figure 6-66(B), the prominent 3 kHz components compare well to those measured in Figure 6-62(B), both with magnitudes of 7 A.



(A) (B)

Figure 6-66: Simulated DC Bus Current FFT Components for the NPCC

6.6.1.4 Investigation Summary

The comparative measurements for harmonic frequencies up to 1500 Hz are summarised in Table 11. Although the SSC, from a visual inspection of the waveforms, appears to contain lower harmonic components those that of the NPCC, the calculated power loss in the electrolytic DC bus capacitors proves to be higher. In Table 11, the power loss in the capacitors for the SSC is represented as a percentage of the power loss in the NPCC. Any variable changes, for example resistance values, would be common to both, ensuring that the percentage loss would remain the same. Although the power levels that both converters operated at are not high, it is evident that when choosing the SSC for any of the traction and MVDC applications, the DC bus capacitor bank would require a higher rating than that of the NPCC.

The simulation results, as were seen in this comparison, provide information on the incidence of various frequency components; however, small errors in the current magnitudes are witnessed. Also evident in the simulations is the absence of many of the lower harmonic components. The difficulty in modelling the magnetic components, i.e. the three-phase inductors, transformers, precise switch models and extra parasitic components, is partly responsible. These are all factors that influence the open-loop modulation of the various waveforms. However, they still provide a useful function in identifying specific components that could potentially become troublesome.

Table 11: Low-Frequency DC Bus Capacitor Current Magnitudes for SSC and NPCC

Frequency Component	SSC Supply I_{DC}=30.4 A		NPCC Supply I_{DC}=32.0 A	
50 Hz	0.0 A		0.35 A	(-49.0 dB)
100 Hz	1.26 A	(-38.0 dB)	1.26 A	(-38.0 dB)
150 Hz	0.0 A		0.79 A	(-42.0 dB)
200 Hz	0.32 A	(-50.0 dB)	0.0 A	
300 Hz	0.41 A	(-37.0 dB)	0.89 A	(-41.0 dB)
350 Hz	0.89 A	(-41.0 dB)	0.22 A	(-53.0 dB)
450 Hz	0.0 A		0.56 A	(-45.0 dB)
500 Hz	0.50 A	(-46.0 dB)	0.0 A	
550 Hz	0.40 A	(-48.0 dB)	0.0 A	
650 Hz	2.0 A	(-34.0 dB)	0.12 A	(-54.0 dB)
700 Hz	0.22 A	(-53.0 dB)	0.0 A	
750 Hz	0.0 A		0.28 A	(-51.0 dB)
900 Hz	0.2 A	(-54.0 dB)	0.0 A	
950 Hz	5.01 A	(-26.0 dB)	0.32 A	(-50.0 dB)
1000 Hz	0.78 A	(-43.0 dB)	0.0 A	
1125 Hz	0.0 A		0.28 A	(-51.0 dB)
1175 Hz	0. 22 A	(-53.0 dB)	0.0 A	
1200 Hz	0.22 A	(-53.0 dB)	0.0 A	
1250 Hz	0.25 A	(-32.0 dB)	0.0 A	
1350 Hz	0.40 A	(-48.0 dB)	0.28 A	(-51.0 dB)
1450 Hz	0.25 A	(-52.0 dB)	0.16 A	(-56.0 dB)
1500 Hz	0.0 A		0.28 A	(-51.0 dB)
% Power Loss	159.63%		100%	

(Note: dB Values as read from measurements – Current Values scaled by 100 to real values)

6.6.2 Inductor Ripple Currents

6.6.2.1 Investigation Criterion

The filter inductors, critical in the task of wave shaping the output waveforms, are the second group of components investigated. In the performance of their task, they are continually subjected to high-frequency ripple current components. These components result in high-frequency losses, which can be broken down into three basic categories. The first of these losses are the copper losses. The resistive element within the copper windings causes heating as a result of the I^2R losses. These losses occur for each of the harmonic frequency components, identical to those experienced in the DC bus capacitors.

The second group of losses are the hysteresis losses. The area enclosed in the hysteresis curve, expressed on a *B-H* (flux density and magnetic field intensity) axis, is the work done on the material by the applied magnetic field. This energy used to perform the work is dissipated within the material, resulting in a rise in temperature, the losses being referred to as hysteresis losses. Furthermore, the hysteresis losses increase with the flux density and the switching frequency that the material is exposed to [68][69]. During high-frequency switch-

ing, the high-frequency hysteresis losses add to the hysteresis losses of the fundamental component, further increasing the heating within the material.

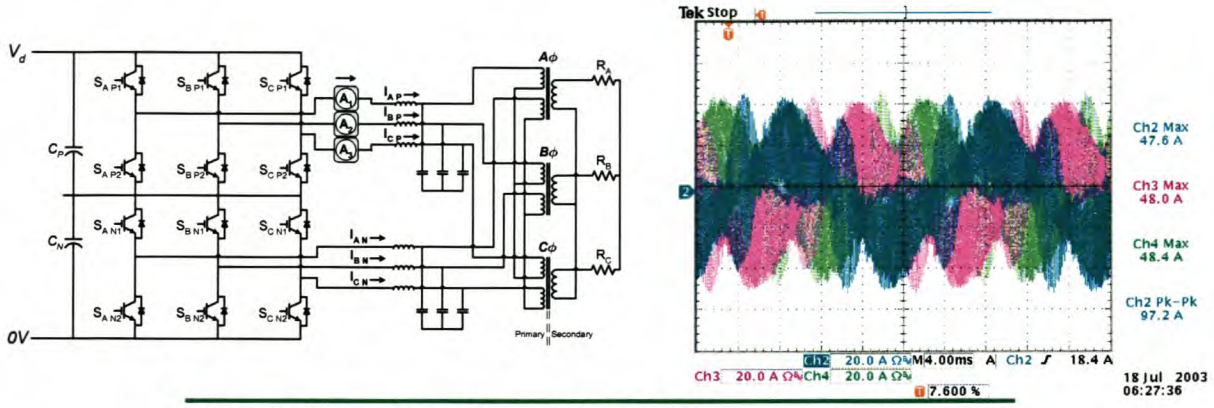
The last of the losses are eddy current losses. Eddy currents are induced in the core and parallel windings of the inductors by the magnetic field generated by the current flowing through the windings. This magnetic field is induced perpendicularly to the direction of the current flow. This results in a current being induced in the core and the conductors, flowing in parallel or in the opposite direction to the current flowing in the conductors. A common technique used on 50 Hz transformers, reducing the core loss, is that of using a laminated steel core. The laminations ensure that a conduction path is not created in the core. With high-frequency currents flowing in the conductors, these laminations act as capacitor plates, creating a low impedance path for the high-frequency components. It is for this reason that steel laminated cores are generally avoided above 2 kHz [68]. Ferrite cores, whose material are of a powdered granular nature, providing the necessary isolation, and have low losses at high frequencies, are usually used. But ferrites are limited to lower power ratings, typically 2 kW, mostly due to the limitations in pressing the cores for large power applications.

With the three basic loss components identified, it can be seen that the effect of all of them is predominantly heating losses in the form of I^2R losses. Overheating ultimately results in the destruction of the magnetic components. In [58] inductive elements are attributed to 6% of failures within switchmode supplies. However, in high power applications steel laminated cores are usually used, resulting in higher losses. The high power inductive elements also become a considerable portion of the overall cost of the converter. Thus operational fatigue to the inductive elements should be avoided at all costs. Therefore in this comparison attention is not given to the specific loss components, but to the current composition of the ripple currents flowing through the inductors. This ultimately provides an indication of which of the topologies applies their inductors to the greatest heating stress.

It should be noted that voltage stresses, increasing the electrical stress and potentially causing insulation breakdown, are not discussed since one of the main motivators for choosing a multilevel topology is to reduce this stress in the first place.

As was the case for the DC bus capacitor investigation, only one of the modules of the SSC is considered, since using normal or interleaved SVM ultimately results in the inductors experiencing the same ripple currents in both the top and bottom converters.

6.6.2.2 Practical SSC Results Using Normal SVM and Interleaved Switching



Measuring Point	Measured Value	Channel on Scope	Description
A_1	I_{AP}	Ch 2	Top Converter's Aϕ Current
A_2	I_{BP}	Ch 3	Top Converter's Bϕ Current
A_3	I_{CP}	Ch 4	Top Converter's Cϕ Current

Figure 6-67: SSC Inductor Ripple Current Measurements

The measured waveforms, flowing through the 100 μH inductors, are represented in Figure 6-67. Large ripple current magnitudes, similar to those shown in section 6.5.2.1, are seen.

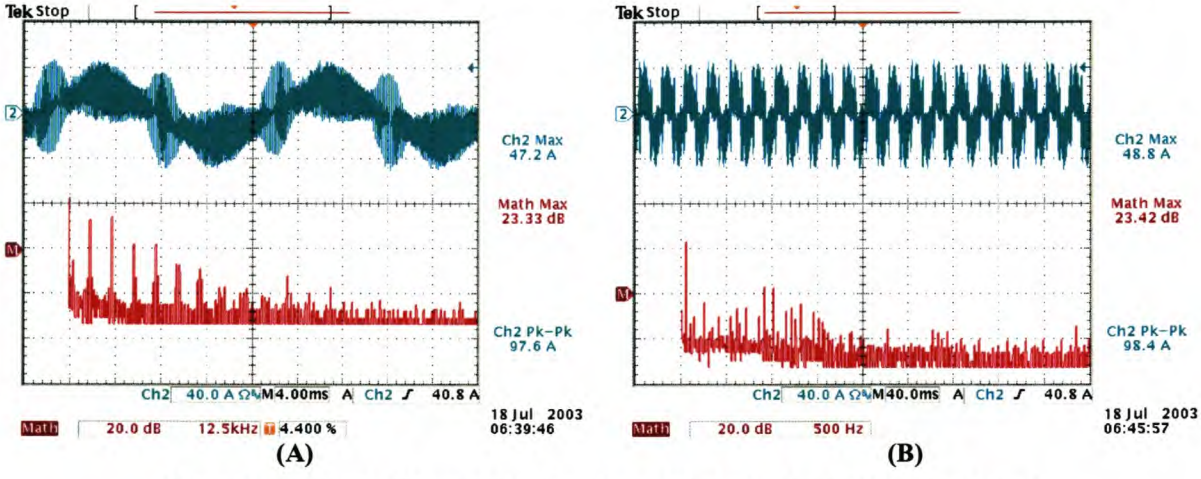


Figure 6-68: Ripple Current flowing through Inductor $L_{Fa\,1}$ (SSC Topology)

High ripple content is observed at the zero crossover points as well as at the crest of the waveform. Maximum values measured indicate peak values of approximately 48 A. One of the phases is considered in Figure 6-68(A&B), where FFTs of the ripple current components are displayed. In Figure 6-68(A) the presence of the high-frequency switching ripple is clearly present, with the largest component being the 12 kHz components, measured as 5.01 A. Alternatively the lower frequency components, Figure 6-68(B), provide an indication of the loading conditions. The largest component measured is, as expected, the 50 Hz component, measuring 14.83 A. Large 19th and 21st harmonics are also present in the measured waveform, approximately 1.58 A.

As discussed in the investigation criterion, specific values provide little information on the effect that the ripple current has on the inductors. A more feasible comparison between the

two topologies is obtained by calculating the THD of the waveforms. The THD encompasses all the measured quantities, switching scheme related and load related, the load being identical in both topologies. Dominant harmonics will affect the THD, and thus the topology with the lowest THD is deemed to impact less on the inductors. Using the MATLAB® routine, Appendix E, a THD of 68.36% was measured.

The simulated waveforms and the respective FFTs are shown in Figure 6-69(A&B). The magnitudes are slightly smaller, measuring peak values of approximately 28-30 A. This is also evident in the FFT results, where the 6 kHz component is approximately the same as in the practical measurement, 4.5 A, and the 12 kHz is approximately 3 A as opposed to the 5 A measured. The simulated 50 Hz component measures 20 A as opposed to the 14.83 A measured practically.

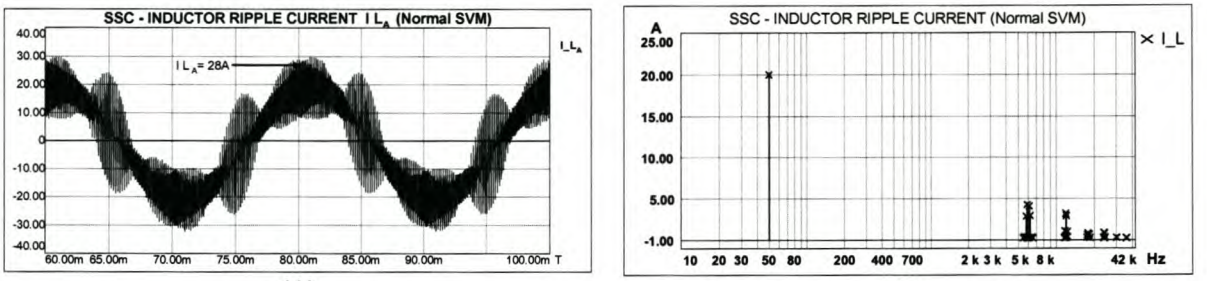
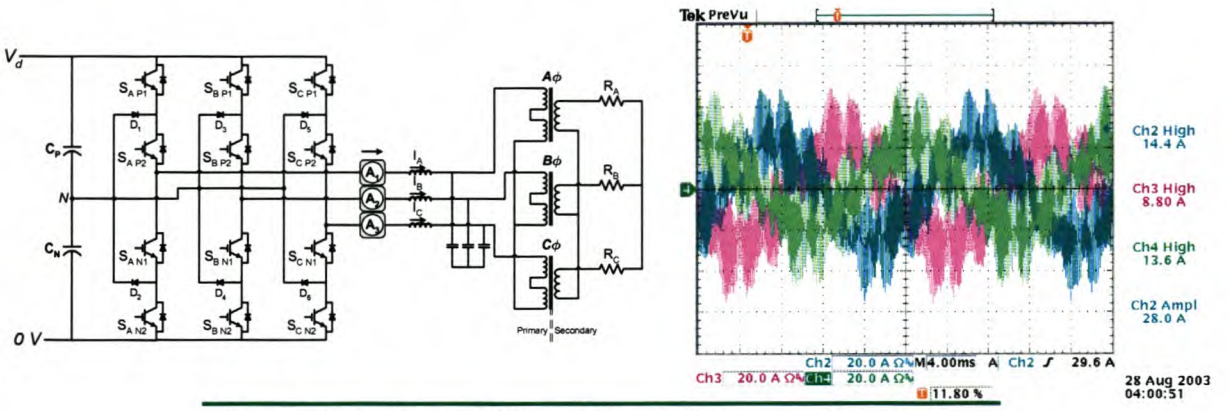


Figure 6-69: Simulated Inductor Current FFT Components for the SSC

With both the simulation model and the practical model operating with exactly the same load parameters, modulation index and DC bus value, the deviation in the simulation results are attributed to transformer, inductor, filter and load variations, difficult to measure on the practical system.

6.6.2.3 Practical NPCC Results Using 3-Level SVM



Measuring Point	Measured Value	Channel on Scope	Description
A_1	I_A	Ch 2	Converter's Aϕ Current
A_2	I_B	Ch 3	Converter's Bϕ Current
A_3	I_C	Ch 4	Converter's Cϕ Current

Figure 6-70: NPCC Inductor Ripple Current Measurements

The measurement points and the measured ripple current flowing through the 200 μH inductors of the NPCC are recorded in Figure 6-70. Evident at first glance is the visible reduction in the ripple current magnitude. Analysing the high-frequency ripple current components, Figure 6-71(A), it is seen that the switching ripple disappear at approximately 36 kHz, as opposed to the 72 kHz seen in Figure 6-68(A). The measurement of the lower frequency components, Figure 6-71(B), indicates the presence of the 3 kHz components, not observed in Figure 6-68(B). Similar to the SSC, the NPCC measurement also indicates a large 19th harmonic component, measured at approximately 1.25 A. Performing a THD on the measured ripple current of the NPCC indicates a 53.3% harmonic distortion. The SSC therefore exposes its inductors to 28% more ripple current than the NPCC.

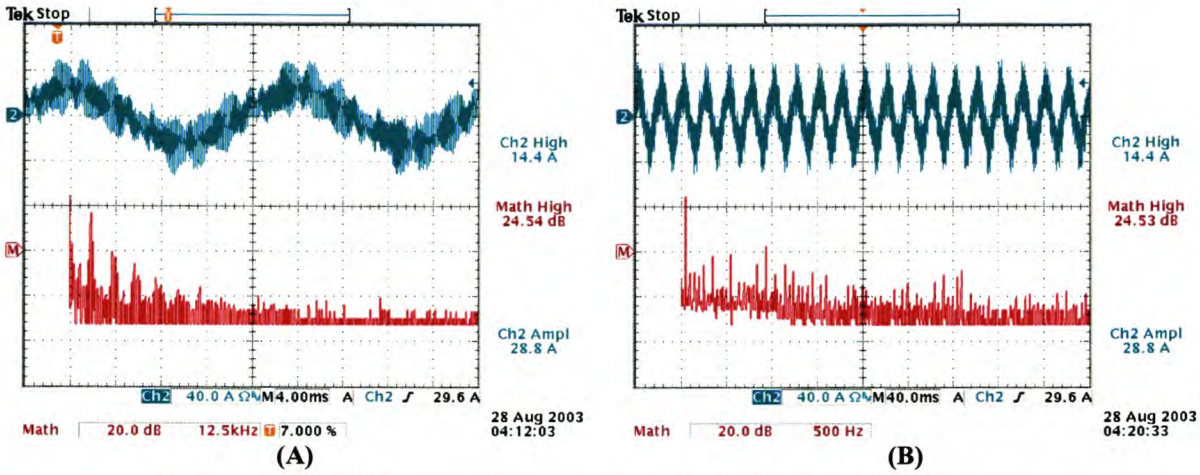


Figure 6-71: Ripple Current flowing through Inductor L_{Fa} (NPCC Topology)

The simulated waveforms yield waveforms with comparable wave shapes, seen in Figure 6-72(A). Once again the magnitudes are observed to be smaller than those measured practically. The measured waveform of the inductor ripple current has a peak amplitude of approximately 30 A, compared to the 40 A peak values in Figure 6-71(A). In the FFT measurement, Figure 6-72(B), the absence of the lower frequency harmonic components is noticeable. However, the switching ripple components, which have a large impact on the wave shape, are clearly visible. As in the measured waveforms in Figure 6-72(A), the 6 kHz components are most dominant.

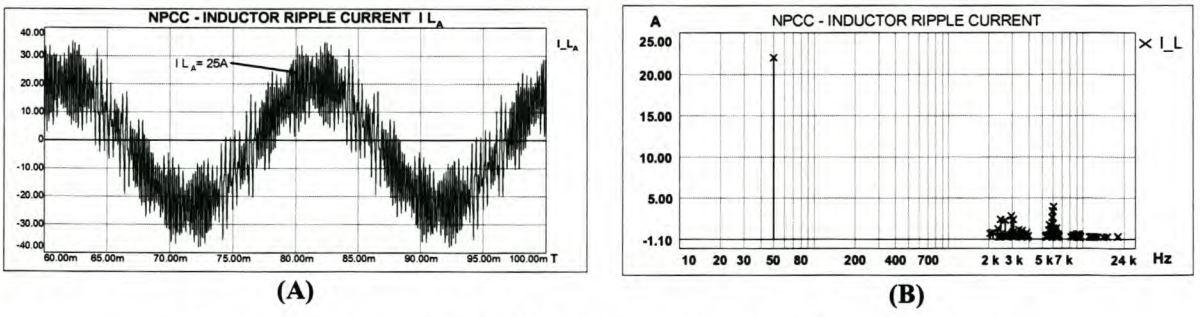


Figure 6-72: Simulated Inductor Current FFT Components for the SSC

The simulations provide insight into the expected practical measurements; however, the absences of modulation harmonics are evidence of the limitations of the simulation model. More accurate simulations require far more accurate components. This is not always practical as the specific values for inductors, transformers and overall system losses are unique to each practical converter. Having said this, the simulation in its present format provides a fair indication of the expected output waveforms and current and voltage components appearing in and over various components.

6.6.2.4 Investigation Summary

The comparative measurement of the ripple currents through the filter inductors identifies the SSC as the topology having the largest loss creating ripple current components. As discussed in the investigation criterion, the losses are all current related. Hysteresis losses, dependent on the flux density and the switching frequency, would be higher than those experienced in the NPCC, a visually obvious deduction when considering the harmonic spectrum of the high-frequency ripple components for both topologies. Eddy current losses are also expected to be higher in the SSC, as they too are frequency dependent. THD values of 68.36% for the SSC and 53.3% for the NPCC confirm these findings.

With the SSC inductor values being 100 μH, and the NPCC having inductor values of 200 μH, a higher ripple current is almost expected. However, the investigation criteria of the topologies require both inverters to have identical impedances. Furthermore, within the SSC each module subjects half of the DC bus voltage to the inductors, whereas in the NPCC, the full DC bus voltages are subjected to the inductors.

This investigation has shown that the inductors of the SSC are required to withstand higher current ripple components and require better cooling than those in the NPCC.

6.7 Chapter Summary

By comparing the practical models of the SSC, using 2-Level SVM, and the NPCC, using the 3-Level SVM it has been possible to determine some performance aspects of the topologies. In Table 12 the hardware requirements and practical performance results of the two topologies are compared.

Measuring the performance has shown that the NPCC offers a solution that is more efficient. This is verified in the measurements of the DC capacitor losses and the high percentage harmonic distortion in the inductor ripple currents, as both measurements are loss related. The NPCC's alternative switching operation also contributes to the efficiency.

While using open-loop control, the quality of the modulated current waveforms within the SSC is of a higher quality. The voltage waveform measurements seem to contradict this. However, the large distortion in its THD is attributed to the 3rd harmonic voltages that are present while switching into a load with the neutral disconnected. Closed-loop control would result in the overall improvement of the current and voltage waveform THDs.

Table 12: Topology Comparisons

Focal points	SSC Values	NPCC Values
Number of IGBTs	12	12
Compulsory Extra Components	Isolation Transformer 3 extra Filter Inductors 3 extra Filter Capacitors (If placed on primary)	6 Extra Diodes
Control Complexity	Low (Normal and Interleaved)	High (3-Level SVM)

Topology Performance:	SSC (Normal SVM)	SSC (Interl. SVM)	NPCC (3-Level SVM)
Load Voltage % THD (With TRFR)	12.61%	9.95%	7.69%
Load Voltage % THD (No TRFR)	5.36%		4.58%
Load Current % THD	2.93%	2.99%	4.21%
Efficiencies	81%	80%	90%
DC Bus Capacitor Stress	Higher than NPCC		Lower than SSC
Percentage Power Loss in Capacitor	59.63% more than NPCC		Lower than SSC
Inductor Currents	High Losses		Lower Losses
Filter Inductor Losses expressed as THD	68.36%		53.3%

Another observation is made of the simulation models. Evident in all the simulation results is the absence of the lower frequency ripple current components. Attributed to the use of ideal components, the practical measurements can be used to improve the simulation performance. Specific target areas are the switches, capacitors, filter inductors and load. The practical assessment has identified that the impact of three-phase, laminated steel core inductors and transformers on the modulation of the waveforms is significant, in both the low and high-frequency range. However, it should also be remembered that simulation models are often used to provide insight and are not necessarily required to be totally accurate. In this regard the simulation models shown have modelled the practically measured waveforms with a fair amount of accuracy.

Chapter 7 Conclusion

Investigation into the performances of the SSC and NPCC topologies has been performed on a number of levels. In the process of determining the characteristics of the two converter topologies, it was shown that the capabilities of the converter based technology offer a far superior solution to general power quality mitigation and transformation than those of the traditional devices. In the quest to perform these functions at higher power ratings, various multilevel converters were evaluated. Ultimately the choice of the SSC and NPCC, selected for comparison, lay in their simplicity and independence of specialised design and implementation constraints. The performance evaluation of each of the topologies is listed on a per-topology basis, and yields the following findings:

7.1 Investigation Summary of the SSC Topology (Normal SVM)

7.1.1 Positive Elements:

- A low complexity control technique and straightforward implementation.
- Natural balancing of DC bus capacitors after transients.
- Dominant switching harmonics appear at 6 kHz and multiples thereof.
- Low voltage stresses, attributed to structure and switching scheme.
- Low %THD load current.
- No extra silicon devices required, only the 12 switches.
- Number of levels easily increased for higher voltage operation.
- Higher quality open-loop waveform modulation.
- Modular converter construction can be used, ensuring lower parasitic components.

7.1.2 Negative Elements:

- High number of passive components (specialised transformer, 3 extra inductors and 3 extra filter capacitors if placed on transformer primary).
- Higher losses in DC bus capacitors than NPCC, thus requiring higher ripple current ratings.
- High %THD in filter inductor current, when compared to NPCC, implying higher losses per inductor for each of the 6 filter inductors.
- Higher switching losses as all 12 switches and their anti-parallel diodes have conduction and switching losses.
- Lower overall efficiency than NPCC, attributed to higher capacitor, inductor and switching losses.
- 3^{rd} harmonic voltage components on output waveform due to transformer connections, need to connect load neutral to transformer which can result in high 3^{rd} har-

monic currents flowing due to load imbalance.

7.2 Investigation Summary of the SSC Topology (Interleaved SVM)

7.2.1 Positive Elements:

- A low complexity control technique slightly more complex in implementation than normal SVM.
- Fastest natural balancing mechanism of DC bus capacitors of all topologies after transients.
- Low voltage stresses, attributed to structure and switching scheme.
- Low %THD load current.
- Dominant switching harmonics appear at 12 kHz and multiples thereof.
- Reduction in filter capacitance possible, due to interleaved switching.
- No extra silicon devices required, only the 12 switches.
- Number of levels easily increased for higher voltage operation.
- Higher quality open-loop waveform modulation.
- Modular converter construction can be used, ensuring lower parasitic components.

7.2.2 Negative Elements:

- High number of passive components (specialised transformer, 3 extra inductors and 3 extra filter capacitors if placed on transformer primary).
- Higher losses in DC bus capacitors than NPCC, thus requiring higher ripple current ratings.
- High %THD in filter inductor current, when compared to NPCC, implying higher losses per inductor for each of the 6 filter inductors.
- Higher switching and conduction losses, identical to SSC using normal SVM.
- Lower overall efficiency than NPCC, attributed to higher capacitor, inductor and switching losses.
- Same transformer constraints as found for SSC using normal SVM.

7.3 Investigation Summary of the NPCC Topology

7.3.1 Positive Elements:

- No extra passive components required than normal.
- Low voltage stresses, attributed to structure and switching scheme, high number of levels in stepped voltage output.
- Lower switching losses attributed to long zero states with only 6 switches operating at the switching frequency, no anti-parallel diode conduction since freewheeling

diodes conduct all freewheeling currents.

- Lowest percentage losses in DC capacitors thus required ripple current ratings are lower.
- Lowest %THD in filter inductors, implying lowest losses for inductors, occurring in a lower number of inductors.
- Highest efficiency of the two topologies, attributed to lower switching, DC capacitor and filter inductor losses.
- Isolation transformer not required.

7.3.2 Negative Elements:

- High complexity control technique, with stability dependant on switch selection sequence.
- Requires 6 extra freewheeling diodes.
- Low %THD load current.
- Waveform modulation quality dependant on switch sequence selection .
- DC bus capacitor unbalancing severely affected by the switching of medium voltage vectors.
- A dominant switching harmonics appears at 3 kHz, requiring low cut-off frequencies of low-pass filters.
- Increase in number of diode clamped output voltage levels is problematic, requires DC bus capacitor charge control.
- Open-loop modulated waveforms have largest %THD of the three topologies compared.
- Parasitic components are more problematic for the NPCC as switches and freewheeling diodes need to be placed in close proximity to the DC bus and each other in order to reduce parasitic elements .

7.4 Overall Summary

The practical comparison serves well to identify specific shortcomings in either of the topologies. While the NPCC proves to be the more efficient topology, it is evident that the modulation process is complex, with DC bus voltage unbalance a far more severe criterion. For the SSC, it is noted that although the efficiency is lower, various other aspects make it an attractive topological choice, for instance its modularity.

Each of the topologies has further merits when considering the application of the converters. An NPCC would tentatively be the converter of choice where a high output voltage, with no transformer, is required, i.e. an in-line active rectifier with regeneration capabilities for traction applications. The SSC would tentatively be more attractive in a shunt or series compensating topology where a transformer is already required. Even though the NPCC compo-

nent count is lower, making it less expensive, the SSC has the advantage of being able to use modular building blocks. These modular blocks are standard converters, with lower complexity, constructed from components that are available in large quantities. It is this low complexity and modularity that makes the SSC an attractive option. By trying to obtain even higher operating voltages, the usage of a five-level diode clamped device would be sought. A variation of the NPCC, able to generate more stepped voltage output levels, is also substantially more complex than that of a 3-level SSC.

7.5 Future Work

Future work should focus on investigations into alternative switching techniques for both topologies. Further optimised switching techniques using the work listed in [59].

Efficiency comparisons need to be performed at higher power levels, while using closed-loop control, mitigating the low %THD in the modulated waveforms.

Creating simulation models, using more accurate component models and modelling of the converter losses with higher accuracy, taking into account the effects of the transformers and inductors using laminated steel cores at the high switching frequencies.

Chapter 8 Bibliography

[1] B.K. Bose; "Energy, Environment, and Advances in Power Electronics"; IEEE Transactions on Power Electronics; vol. 15, no. 4, July 2000, pp.688-701.

[2] T.G. Wilson; "The Evolution of Power Electronics"; IEEE Transactions on Power Electronics, vol. 15, no. 3, May 2000, pp.439-446.

[3] H. Akagi; "Prospects and Expectations of Power Electronics in the 21st Century"; Proceedings of the Power Conversion Conference; IEEE PCC-Osaka; April 2002, pp.921-926.

[4] B.K. Bose; "Power Electronics and Motor Drives – Recent Technology Advances"; Proceedings of the International Symposium of Industrial Electronics; IEEE ISIE-L'Aquilla; July 2002, pp.22-25.

[5] E.I. Carroll; "Power Electronics for Very High Power Applications"; Power Electronics and Variable Speed Drive Conference; IEE/PEVD; London; September 1998.

[6] H. Stemmler; "High Power Electronics State of the Art and Future Trends"; Power Electronics and Electrometrology Laboratory Publication; Swiss Federal Institute of Technology (ETH); Zurich; 2002.

[7] T.A. Meynard, H. Foch; "Multi-Level Conversion: High Voltage Choppers and Voltage-Source Inverters"; IEEE Power Electronics Specialists Conference; June 1992; pp.397-403.

[8] A. Nabae, I. Takahashi, H. Akagi; "A New Neutral-Point-Clamped PWM Inverter"; IEEE Transactions on Industry Applications, vol. IA-17, no. 5, September/October 1981, pp.518-523.

[9] P.W. Hammond; "A New Approach to Enhance Power Quality for Medium Voltage AC Drives"; IEEE Transactions on Industry Applications, vol. 33, no. 1, January/February 1997, pp.202-208.

[10] J. Kuang, B.T. Ooi; "Series Connected Voltage-Source Converter Modules for Force-Commutated SVC and DC Transmission"; IEEE Transactions on Power Delivery, vol. 9, no. 2, April 1994, pp.977-983.

[11] P.R. Palmer, A.N. Githiari; "The Series Connection of IGBTs with Optimised Voltage Sharing in the Switching Transient", Proceedings IEEE PESC'95, vol. 1, pp. 44-49.

[12] F. Engelbrecht, H.J. Beukes; "Analysis of AC and DC Transmission at Distribution Voltage Levels"; Proceedings of the IASTED International Conference; Power and Energy Systems; IASTED PES 2001; Rhodes; Greece; 3-6 July 2001; pp.233-238.

[13] U. Axelsson, A. Holm, C. Liljegren, M. Aberg, K. Eriksson, O. Tollerz; "The Gotland HVDC Light Project-Experiences from Trial and Commercial Operation"; Electricity Distribution 2001; Part 1: Contributions. CIRED. 16th International Conference and Exhibition; (IEE Conf. Publication No.482); Volume: 1; 2001; Page(s): 5 pp; vol.1.

[14] A.D. Castro, R. Ellström, Y.J. Häfner, C. Liljegren; "Co-Ordination of Parallel AC-DC Systems for Optimum Performance"; Paper presented at the Power Delivery Conference; Madrid, Spain; September 1999, From ABB Power Transmission Website: http://www.abb.com/powersystems.

[15] L. Malesani, L. Rossetto, P. Tenti, P. Tomasin; "AC/DC/AC PWM Converter with Reduced Energy Storage DC Link"; IEEE Transactions on Industry Applications, vol. 31, no. 2, March/April 1995, pp.287-292.

[16] B. Singh, K. Al-Haddad, A. Chandra; "A Review of Active Filters for Power Quality Improvement"; IEEE Transactions on Industrial Electronics, vol. 46, no. 5, October 1999, pp.960-971.

[17] M. Depenbrock, V. Staudt, H. Wrede; "A Concise Assessment of Original and Modified Instantaneous Power Theory Applied to Four-Wire Systems"; Proceedings of the Power Conversion Conference 2002; PCC Osaka 2002; 2002; Vol. 1; pp. 60 –67.

[18] L.M. Tolbert, T.G. Habetler; "Comparison of Time-Based Non-Active Power Definitions for Active Filtering"; Proceedings of the VII IEEE International Power Electronics Congress; CIEP; 2000; pp.73-79.

[19] H. Akagi; "Active and Hybrid Filters for Power Conditioning"; Proceedings of the IEEE International Symposium of Industrial Electronics; ISIE 2000; 2000; vol. 1; pp. TU26- TU36.

[20] H. Akagi; "Trends in Active Power Line Conditioners"; IEEE Transactions on Power Electronics; vol. 9; no. 3; May 1994; pp.263-268.

[21] F.Z. Peng, J-S. Lai; "Application Considerations and Compensation Characteristics of Shunt Active and Series Active Filters in Power Systems"; in Proc. of ICHQP; Las Vegas; NV; Oct. 1996; pp 12-20.

[22] F.Z. Peng; "Harmonic Sources and Filtering Approaches"; IEEE Industry Applications Magazine; July/August 2001; pp 18-25.

[23] J.W. Dixon, G. Venegas, L.A. Moran; "A Series Active Power Filter Based on a Sinusoidal Current-Controlled Voltage-Source Inverter"; IEEE Transactions on Industrial Electronics; vol. 44; no. 5; Oct 1997; pp.612-620.

[24] G. Joós, R. Espinoza; "Three-Phase Series var Compensation Based on a Voltage-Controlled Current Source Inverter with Supplemental Modulation Index Control"; IEEE Transactions on Power Electronics; vol. 14; no. 3; May 1999; pp.587-598.

[25] H. Fujita, H. Akagi; "The Unified Power Quality Conditioner: The Integration of Series- and Shunt-Active Filters"; IEEE Transactions on Power Electronics; vol. 13; no. 2; March 1998; pp.315-322.

[26] G.B. Lee, F. Engelbrecht, H.J. Beukes; "Series-stacked and neutral point clamped multilevel converter topologies for MVDC transmission"; in Proc. of 2002.IEEEAFRICON; Africon 6th Conference in Africa; vol.2; October 2002; pp.735-741.

[27] P.R. Palmer, A.N. Githiari; "The Series Connection of IGBTs with Active Voltage Sharing"; IEEE Transactions on Power Electronics; vol. 12; no. 4; July 1997; pp.637-644.

[28] J. Courault, O. Lapierre, J.L. Pouliquen; "Industrial Interest of Multilevel Converters"; EPE 99 European Power Electronics Conference pdf-format EPE-CD.

[29] S. Bell, J. Sung; "Will Your Motor Insulation Survive a New Adjustable-Frequency Drive?"; IEEE Transactions on Industry Applications, vol. 33, no. 5, September/October 1997, pp.1307-1311.

[30] N. Aouda, L. Prisse, T.A. Meynard, H. Foch; "A Multilevel Rectifier with Unity Power Factor and Sinusoidal Input Current for High Voltage Applications"; EPE Journal, vol. 6 no. 3-4, December 1996, pp.27-35.

[31] T.A. Meynard, M. Fadel, N. Aouda; "Modeling of Multilevel Converters"; IEEE Transactions on Industrial Electronics, vol. 44, no. 3, June 1997, pp.356-364.

[32] F. Hamma, T.A. Meynard, F. Tourkhani, P. Viarouge; "Characteristics and Design of Multilevel Choppers"; IEEE PESC95 Power Electronics Specialists Conference; June 1995; pp.1208-1214.

[33] G. Walker, G. Ledwich; "Bandwidth Considerations for Multilevel Converters"; IEEE Transactions on Power Electronics, vol. 14, no. 1, January 1999, pp.74-81.

[34] Nikolaus P. Schibli, Tung Nguyen, Alfred C. Rufer; "A Three-Phase Multilevel Converter for High-Power Induction Motors"; IEEE Transactions on Power Electronics, vol. 13, no. 5, September 1998, pp.978-986.

[35] J. Rodriguez, L. Moran, A. Gonzalez, C. Silva; "High Voltage Multilevel Converter with Regeneration Capability"; Power Electronics Specialists Conference PESC 99; pp. 1077-1082.

[36] Fang Zeng Peng, Jih-Sheng Lai; "Dynamic Performance and Control of a Static Var Generator Using Cascade Multilevel Inverters"; IEEE Transactions on Industry Applications, vol. 33, no. 3, May/June 1997, pp.748-755.

[37] Fang Zeng Peng, Jih-Sheng Lai, J McKeever; "Multilevel Voltage Source Inverters with Separate DC Sources for Static Var Generation"; IEEE Transactions on Industry Applications, vol. 32, no. 5, September/October 1996, pp.1130-1138.

[38] L.M. Tolbert, F.Z. Peng, T. Cunnyngham, J.N. Chiasson; "Charge Balance Control Schemes for Cascade Multilevel Converter in Hybrid Electric Vehicles"; IEEE Transactions on Power Electronics, vol. 49, no. 5, October 2002, pp.1058-1064.

[39] R. Rojas, T. Ohnishi, T. Suzuki; "PWM Control Method for a Four-Level Inverter"; IEE Proceedings – Electrical Power Applications; vol. 142, no. 6, November 1995, pp. 390-396.

[40] C. Hochgraf, R.H. Lasseter; "A Transformer-Less Static Synchronous Compensator Employing a Multilevel Inverter"; IEEE Transactions on Power Delivery; vol. 12, no. 2, April 1997, pp.881-887.

[41] Lee, Suh and Hyun; "A Novel PWM Scheme for a Three-Level VSI with GTO Thyristors"; IEEE Transactions on Industry Applications, vol. 32, no. 2, March/April 1996, pp.260-268.

[42] B. Mwinyiwiwa, Z. Wolanski, B.T. Ooi; "Current Equalization in SPWM FACTS Controllers at Lowest Switching Rates"; IEEE Transactions on Power Electronics, vol. 14, no. 5, September 1999, pp.900-905.

[43] H. Akagi, Y. Kanazawa, A. Nabae; "Instantaneous Reactive Power Compensators Comprising Switching Devices without Energy Storage Components"; IEEE Transactions on Industry Applications; Vol. 1A-20; NO. 3; May/June 1984; pp.625-630.

[44] Yo-Han Lee, Bum-Seok Suh, Dong-Seok Hyun; "A Novel PWM Scheme for a Three-Level Voltage Source Inverter with GTO Thyristors"; IEEE Transactions on Industry Applications; Vol. 32, NO. 2, March/April 1996.

[45] M.J. Ryan, R.D. Lorenz, R.W. De Donker; "Modeling of Multileg Sine-Wave Inverters: A Geometric Approach"; IEEE Transactions on Industrial Electronics; Vol. 46 NO. 6, December 1999.

[46] N. Celanovic, D. Boroyevich; "A Comprehensive Study of Neutral-Point Voltage Balancing Problem in Three-Level Neutral-Point-Clamped Voltage Source PWM Inverters"; IEEE Transactions on Power Electronics; Vol. 15, NO. 2, March 2000.

[47] D. Zhou, D. Rouaud; "Experimental Comparisons of Space Vector Neutral Point Balancing Strategies for Three-Level Topology"; IEEE Power Electronics Specialists Conference PESC; pp.1071-1076, 1999.

[48] L. Malesani, P. Tomasin, V. Toigo; "Space Vector Control and Current Harmonics in Quasi-Resonant Soft-Switching PWM Conversion"; IEEE Transactions on Industry Applications; Vol. 32, No. 2, March/April 1996.

[49] J. Kuang, J. Kuang, X. Wang, B.T. Ooi; "Forced Commutated HVDC and SVC Based on Phase-Shifted Multi–Converter Modules"; IEEE Transactions on Power Delivery, vol. 8, no. 2, April 1993, pp.712-718.

[50] B. Mwinyiwiwa, Z. Wolanski, B.T. Ooi; "Microprocessor-Implemented SPWM for Multiconverters with Phase-Shifted Triangle Carriers"; IEEE Transactions on industry Applications, vol. 34, no. 3, May/June 1998, pp.487-494.

[51] B. Mwinyiwiwa, Z. Wolanski, B.T. Ooi; "UPFC Using Multiconverter Operated by Phase-Shifted Triangle Carrier SPWM Strategy"; IEEE Transactions on Industry Applications, vol. 34, no. 3, May/June 1998, pp.495-500.

[52] B. Mwinyiwiwa, Z. Wolanski, B.T. Ooi; "Current Equalization in SPWM FACTS Controllers at Lowest Switching Rates"; IEEE Transactions on Industry Applications, vol. 14, no. 5, September 1999, pp.900-905.

[53] H. du T Mouton, J.H.R. Enslin; "A High power IGBT based series injection Power Quality Conditioner:" Proceedings of the International Conference on Harmonics and Power Quality, Vol. 1, October 1998, pp.203-209.

[54] H. du T Mouton, J.H.R. Enslin, H. Akagi; "Natural Balancing of Series-Stacked Power Quality Conditioners:" IEEE Transactions on Power Electronics, Vol. 18, no. 1, January 2003, pp.198-207.

[55] S. Ogasawara and H. Akagi; "Analysis of Variation of Neutral Point Potential in Neutral-Point-Clamped Voltage Source PWM Inverters"; Conference Record of the IEEE-IAS Annual Meeting, IEEE Transactions on Industry Applications; Vol. 2; Oct. 1993; pp. 965-970.

[56] H. du Toit Mouton; "Natural Balancing of Three-Level Neutral-Point-Clamped PWM Inverters" IEEE Transactions on Industrial Electronics, Vol. 49, no. 5, October 2002, pp.1017-1025.

[57] K. Harada, A. Katsuki and M. Fujiwara; "Use of ESR for Deterioration Diagnosis of Electrolytic Capacitors"; IEEE Transactions on Power Electronics; October 1; 1993; Volume 8; pp355-361.

[58] P. Venet, F. Perisse, M.H. El-Husseini and G. Rojat; "Realization of a Smart Electrolytic Capacitor Circuit" Industry Applications Magazine; IEEE; Vol. 8; Issue: 1; Jan.-Feb 2002; pp. 16-20.

[59] D.G.Holmes, B.P. Magrath and T. Lipo; "Optimized Space Vector switching Sequences for Multilevel Inverters"; In Proceedings IEEE APEC'2001, Anaheim, CA, Mar.4-8, 2001, pp. 1123-1129.

[60] S. Austen Stigant and A.C. Franklin; "The JSP Transformer Book"; London; Newness-Butterworths; 1973, pp. 609-639.

[61] Peter Vas; "Vector Control of AC Machines"; Oxford Science Publications; Clarendon Press; Oxford; 1990.

[62] Charles.V. Jones; "The Unified Theory of Electrical Machines"; London; Butterworth & Co. (Publishers) Ltd.; 1967.

[63] E. Clarke; "Circuit Analysis of A-C Power Systems – Volume I: Symmetrical and Related Components"; London; John Wiley and Sons Inc. (Publishers), 1943.

[64] E. Clarke; "Circuit Analysis of A-C Power Systems – Volume II"; London; John Wiley and Sons Inc. (Publishers), 1950.

[65] T.L. Skvarenina; "The Power Electronics Handbook, Industrial Electronics Series"; Boca Raton, Florida, CRC Press LCC; 2002,

[66] D.W. Novotny, T.A. Lipo; "Vector Control and Dynamics of AC Drives"; Oxford U.K.: Oxford University Press; 1997.

[67] P. Horowitz, W. Hill; "The art of electronics" Second Edition; Cambridge University Press; pp.371-372.

[68] N. Mohan, T.M. Undeland, W.P. Robbins; "Power Electronics: Converters, Applications and Design"; Second Edition; John Wiley & Sons; New York; 1989.

[69] S.A. Nasar; "Electric Energy Systems"; Prentice Hall; Upper Saddle River; New Jersey; 1996.

[70] H.d.T. Mouton; "Analysis and Synthesis of a 2 MVA Series-Stacked Power-Quality Conditioner"; Ph.D. Thesis; University of Stellenbosch, December 1999.

[71] C. Mostert; "The Analysis, Design and Implementation of a Constant THD Current Controller for Active AC/DC Converters"; Thesis presented for the fulfilment of a Masters Degree in Electrical Engineering at the University of Stellenbosch; December 1997.

[72] D.D. Bester; "Control of a Series Compensator for Power Quality Conditioner"; Thesis presented for the fulfilment of a Masters Degree in Electrical Engineering at the University of Stellenbosch; March 1999.

[73] C. Putter; "Development of a High-Voltage Converter for a DC Machine Drive Application"; Thesis presented for the fulfilment of a Masters Degree in Electrical Engineering at the University of Stellenbosch; December 1997.

[74] G.B. Lee; "The Analysis and Testing of a Three-Level Diode Clamped Converter"; Thesis presented for the fulfillment of a P.D.E. in Electrical Engineering at the University of Stellenbosch; December 2000; pp. 28-45.

[75] D. Drennan; "An Experimental Investigation into Natural Balancing of Three Level Neutral Point Clamped Multi-Level Inverters ";B.Eng Final Year Thesis; University of Stellenbosch; November 2001.

[76] C. Gerhardt "The Development of a STATCON Training Tool"; Final Year Thesis; Fachhochschule Dortmund; Elektrische Energietechnik; January 1999.

[77] M. Bierhoff; "Simulation of a power conditioner for a 3 kV DC traction substation"; Final Year Thesis; Fachhochschule Dortmund; Elektrische Energietechnik; March 2001.

[78] P. Randewijk; "An Overview of Space Vector PWM"; Technical Report; November 1998

[79] Aluminium Electrolytic Capacitors Data book; Itelcond; 1997.

[80] Aluminium Electrolytic Capacitors Application Notes; BHC Components; EVOX RIFA Group; www.bhc.co.uk.

Appendix A SIMPLORER® Simulation Models

A.1 Model for the Series-Stacked Converter – Normal SVM Switching

Normal SVM for the 2-level SSC is implemented using the simulation package SIMPLORER®. The simulation involves the graphical modelling of the converter topology using the Internal Schematic tool, the model seen in Figure A-1. Two DC sources are used to supply the DC busses of the individual converters. The outputs of each of the three-phase converters are switched into individual isolation transformers. Voltage isolation is achieved in this way, while the output connections ensure that the individual components sum to form the three-winding transformer. The load is a resistive load.

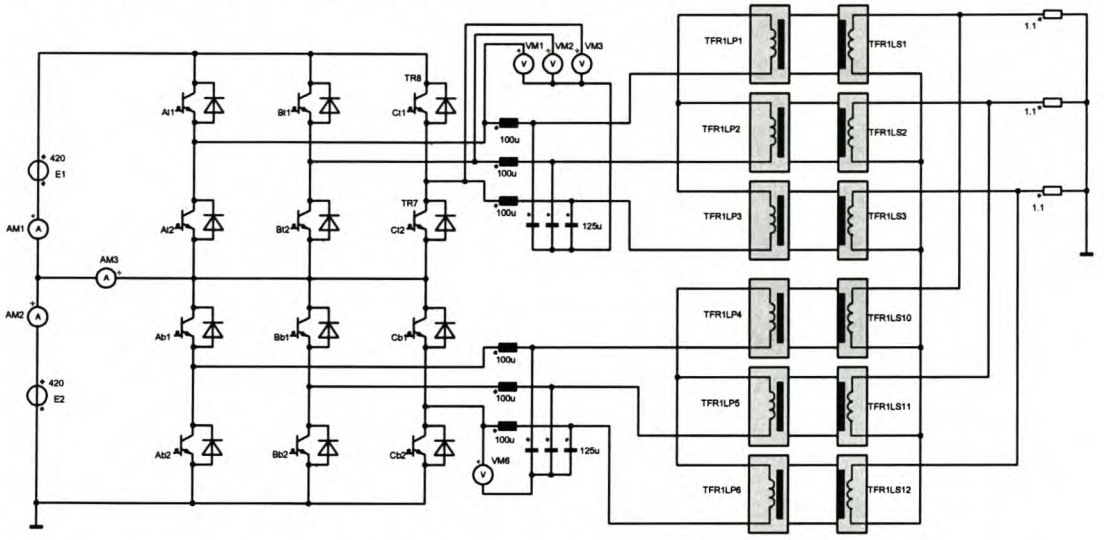


Figure A-1: Normal SVM - SSC Graphical Model

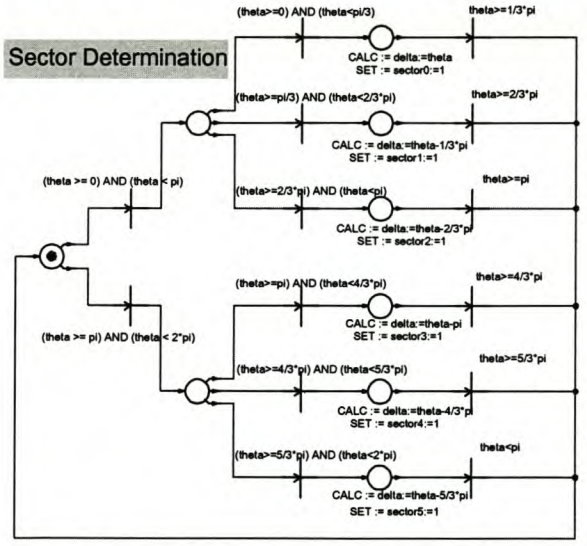


Figure A-2: Normal SVM - Sector Determination Process

A p.u. Reference vector, V_{ref}, is specified in terms of m_a, and is rotated through 360°. The step angle θ is a function of the switching and fundamental frequencies. Determination of the

relevant sector that V_{ref} is situated in is performed using the state graph modules seen in Figure A-2. The process is started at the state with the dot in it. The size of θ is determined, and the sector that it lies in, is selected and latched until V_{ref} passes one of the switching state boundaries, located every 60°. The process then loops around and a new sector is selected. With the sector selected, θ is referred back to sector 0 and renamed δ. Each time θ steps, δ is updated, until θ reaches the switching state boundary of its current sector selection and the process re-starts.

Occurring at the same time as the sector determination, the duty cycles are calculated, using the state graphs seen in Figure A-3. The duty cycles are zero assigned after each calculation. Seen also is the usage of δ in the calculations.

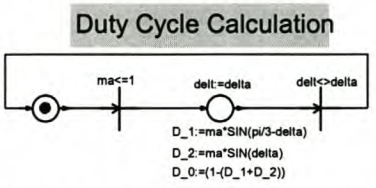


Figure A-3: Normal SVM - Duty Cycle Calculation

The results of these two processes are used to determine the switching states the process of which can be seen in Figure A-4.

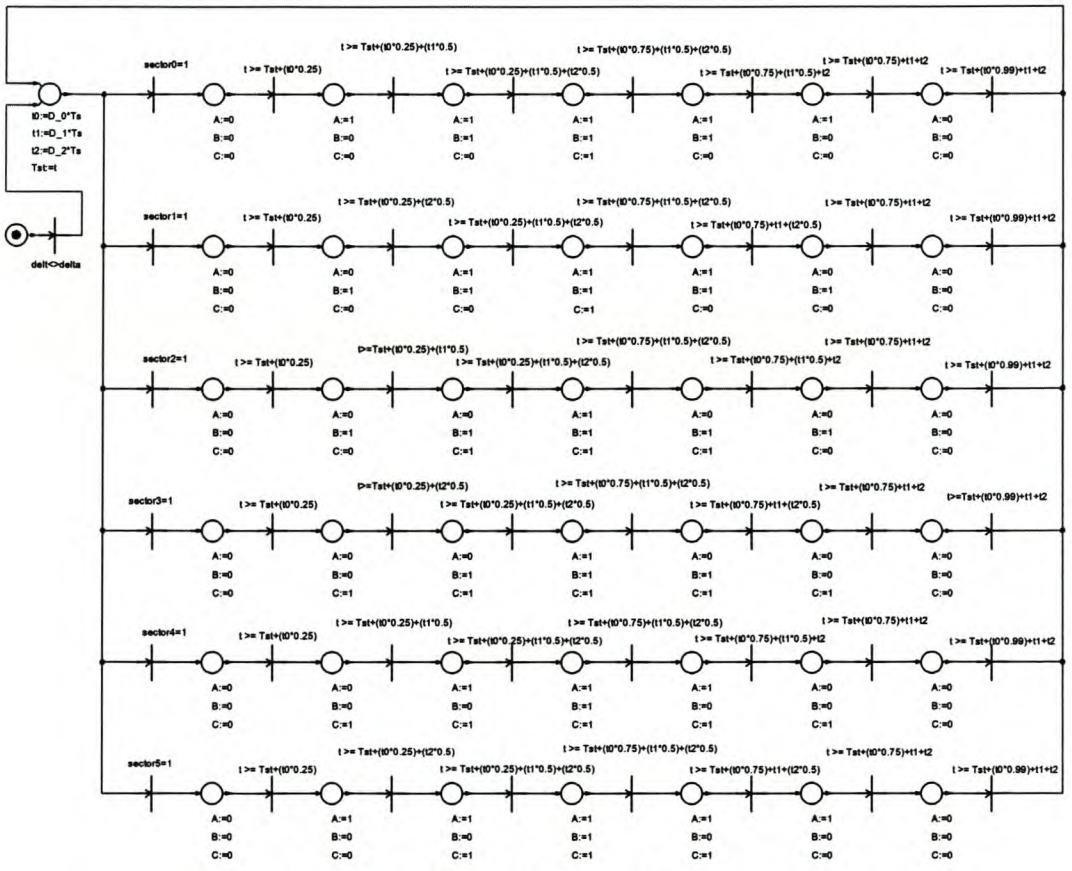


Figure A-4: Normal SVM - Switch State Selection Process.

The process is once again initiated by setting up the initial conditions, seen in the first state element. Here the duty cycles are converted from a percentage of the switching time to a real

time based value. Thereafter the sector that has been selected, by the previously mentioned processes, will initiate the selection of the switch states for their desired duration. When state A is set equal to 1, then the A-phases of both converters are required to be set to a P state, i.e. the top switch of each of the A-phases is required to be closed.

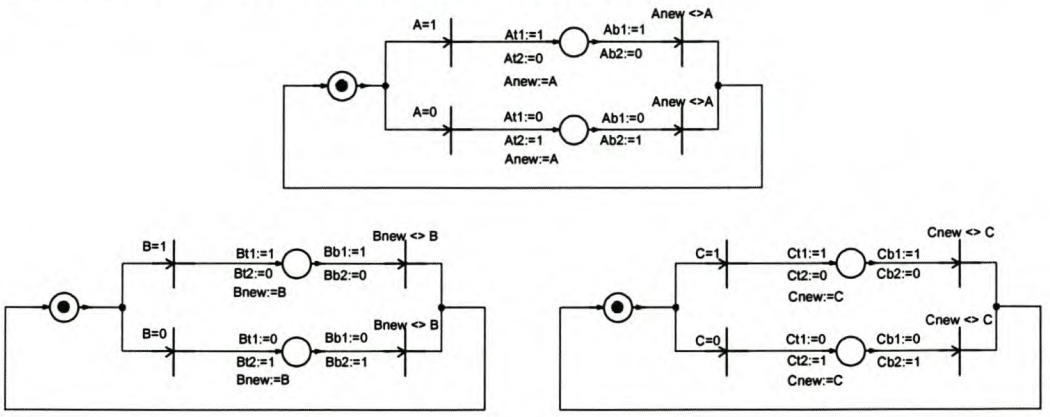


Figure A-5: Normal SVM - Gate Drive Selection and Multiplexing Process.

To enable this the state graph module seen in Figure A-5 is used. The signals are multiplexed and sent to the gates of both converters making up the series-stacked converter. Initiating these states permits the successful simulation of the Series-Stacked Converter using normal SVM.

A.2 Model for the Series-Stacked Converter – Interleaved SVM Switching

The interleaved SVM simulation technique was implemented using the SSC graphical model seen in Figure A-6.

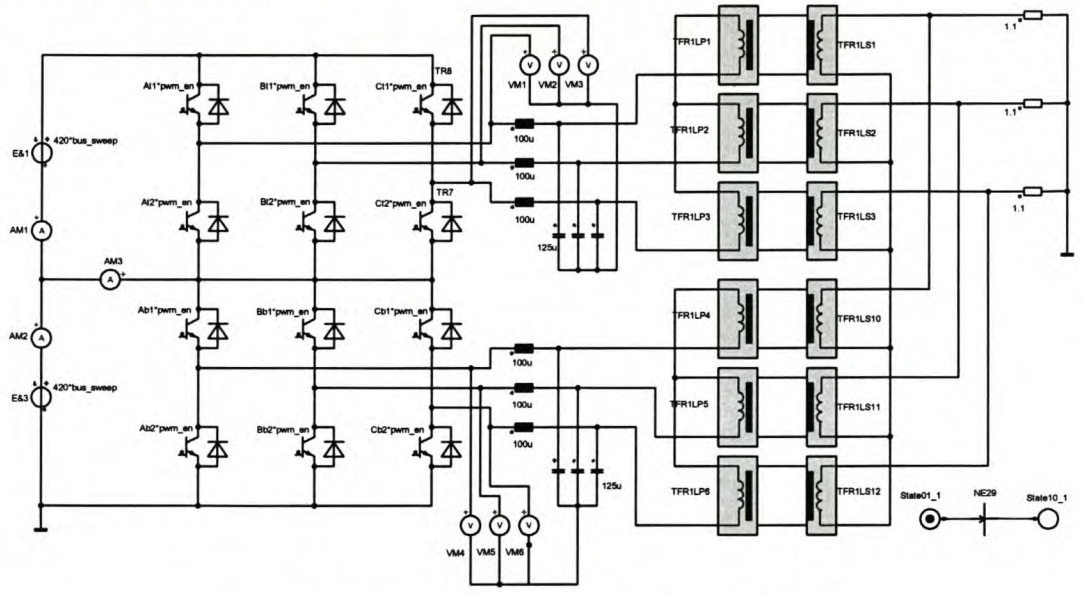


Figure A-6: Interleaved SVM - SSC Graphical Model

The major difference to the previously discussed simulation model is that of the addition of

a phase-shifted carrier in the simulation. The application of the extra carrier is seen in Figure A-7. Making use of saw tooth timing function modules generates each carrier. The operation of one of the modules is to be discussed first. An angle, θ, is generated and kept constant throughout one switching period. This is done by allowing the saw tooth waveform, which counts up to a numerical value of 166.6μs, to latch the angle θ after 10μs into its count. The phase of Fsw2 is set 180° out of phase to that of Fsw, thereby creating the phase shifting required for interleafing.

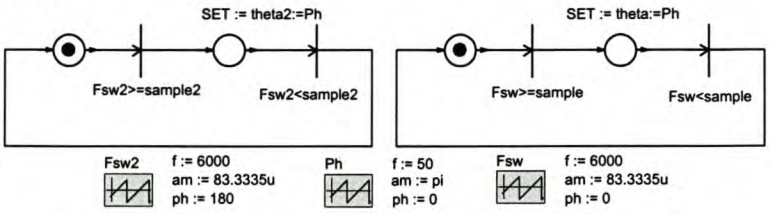


Figure A-7: Interleaved SVM - Phase Shifting of Carrier

Two angles are generated, θ and θ_2, and sent to two separate sector-determining modules, each identical to that seen in Figure A-2. With the angles generated, a common modulation index can be chosen for V_{ref} and sent to the duty cycle generating modules, both being identical to that seen in Figure A-3. Using the appropriate formulas, the calculated duty cycles are sent to the switching state selection processes. The same modules as seen in Figure A-4 are used, with the exception that their outputs are designated x and x_2, where x = phases A, B&C.

The next step is to select the correct switches after the switching times are determined, and this is performed using the converter gate drive selection module seen in Figure A-8.

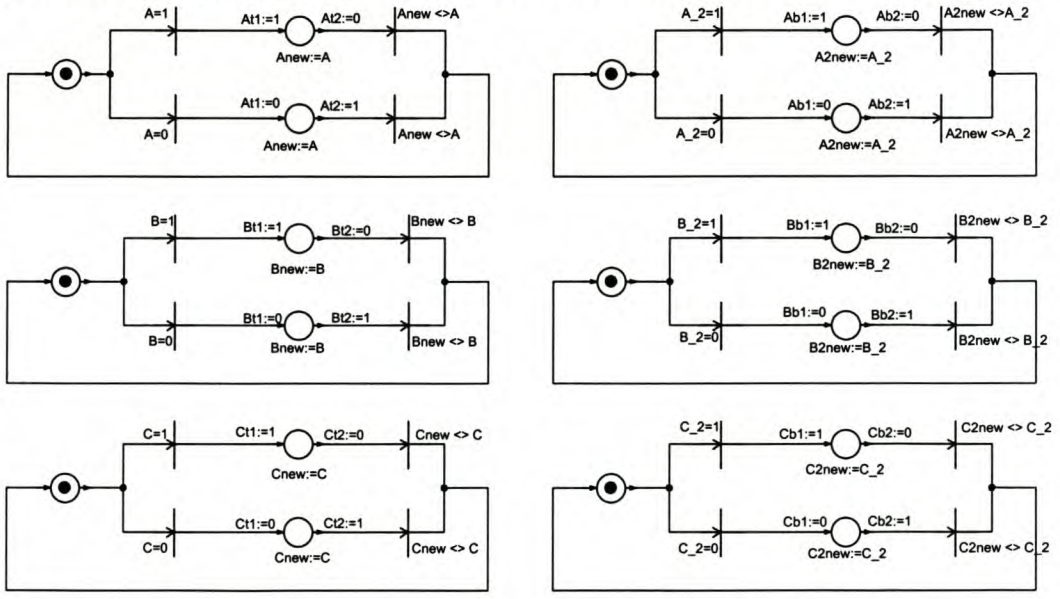


Figure A-8: Interleaved SVM - Converter Gate Drive Selection

These gating pulses are then sent to the graphical model, Figure A-6, and the simulation is run.

A.3 Model for the Neutral Point Clamped Converter 3-level SVM Implementation

Implementation of the calculated quantities, of sections 5.3.1.1 and 5.3.1.2 , into the simulation model followed the following process. A 3-level NPC converter model, Figure A-9, was created using the graphical interface of the SIPMLORER® package. The simulation parameters, listed in Table 6, were used.

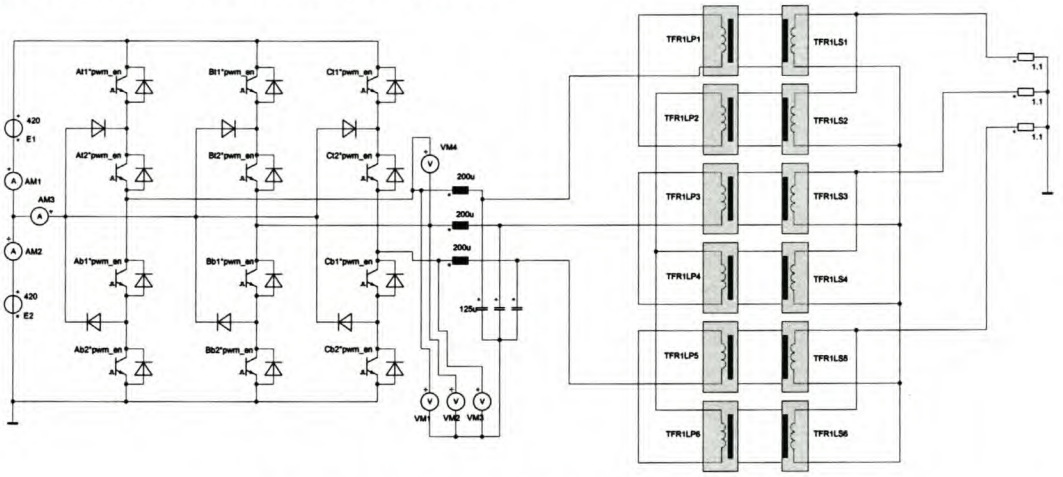


Figure A-9: The 3-Level NPCC Simulation Model

The V_{ref} was again expressed in terms of m_a, a p.u value. The reference vector, like before, is stepped through 360° in step sizes equal to the fundamental frequency divided by the switching frequency multiplied with 360°, performed by the state machine shown in Figure A-10.

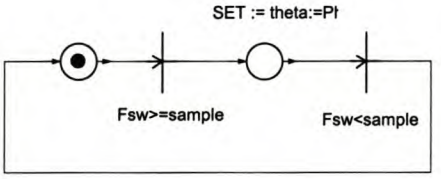


Figure A-10: 3-Level SVM Reference Generator

As was the case for the 2-level SVM method of sector determination, the 3-level SVM uses the same method for this process. The process is shown in Figure A-11. The angle θ is again rotated back into the first sector, made possible because of the circular symmetry of the switching vectors. The sector in which the reference vector is located in, determines the angle magnitude subtracted from the angle θ. This process provides the next process with the size of the angle δ, as well as flagging the relevant sector as active, another state used later in the 3-level SVM process.

In Figure A-11 the sector selection is reset to equal zero, once the angle θ has been incremented past the limiting boundaries. This is observed on the far right of the figure. As the boundary is passed the next sector can be selected, depending on the size of the angle. This

process is flexible enough that it can compensate for any sudden changes in the reference angle. This condition would typically arise when non-linear waveforms have to be modulated.

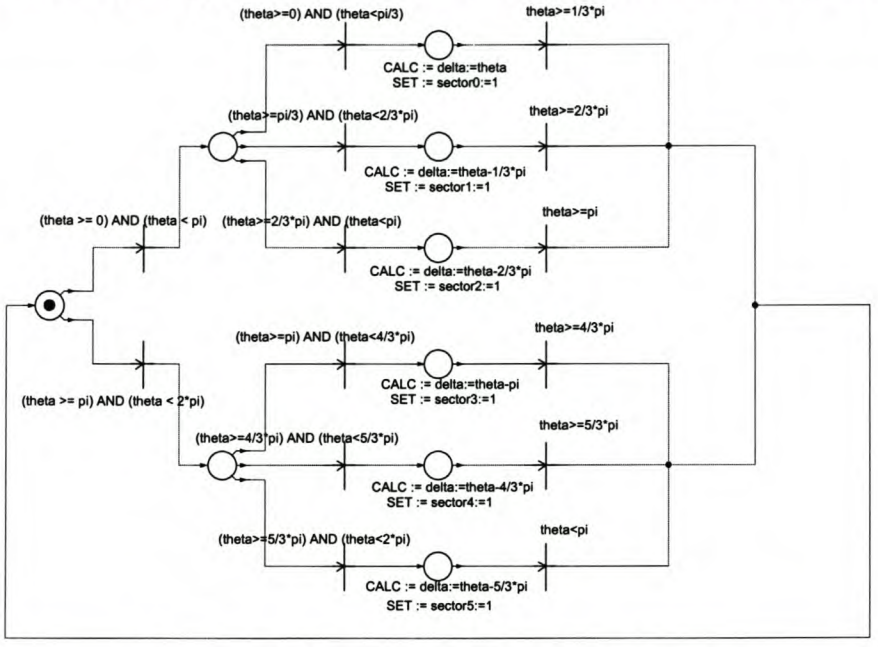


Figure A-11: 3-Level SVM Sector Detection Process

Unlike 2-level SVM, the 3-level SVM control strategy requires the knowledge of the regional positioning of the reference vector, as discussed when deriving the boundary condition equations (5.17) to (5.20). These equations are implemented into the simulation model using the process depicted in Figure A-12, which is identified within the simulation as the regional selection criteria.

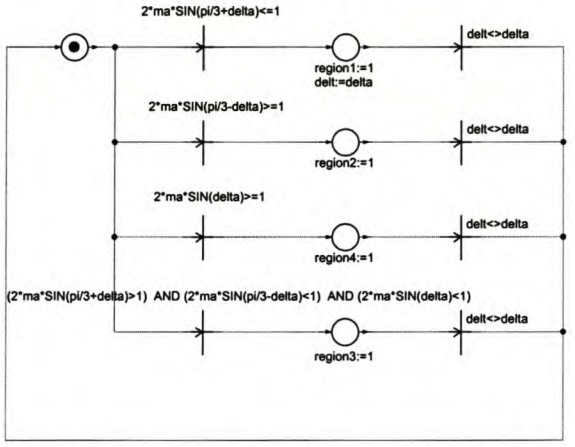


Figure A-12: 3-Level SVM Region Determination Process

Region 3, as discussed when deriving the formulae, is defined by the reference vector not conforming to any of the conditions of the three other regions.

With the correct region selected, the simulation uses the process seen in Figure , for the implementation of the duty cycles in each region. This process requires the regional selection from the process in Figure A-13, and thereafter it calculates the required duty cycles.

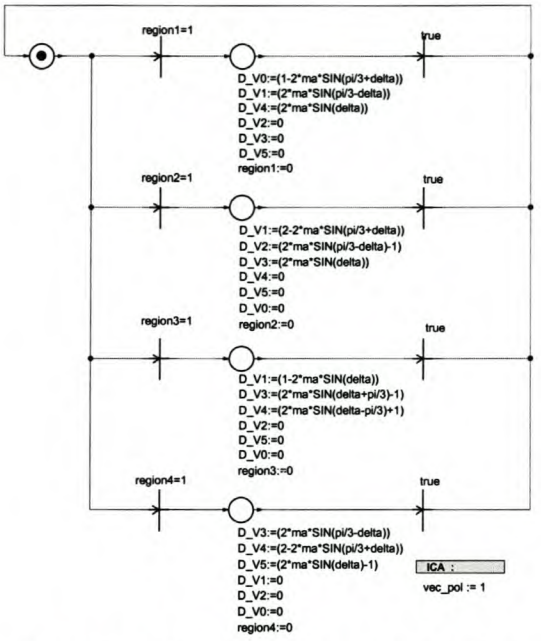


Figure A-13: 3-Level SVM Duty Cycle Calculation Process

This process then sends the appropriate duty cycles to the process seen in Figure A-14. Although rather busy, this process selects the required switching state, depending on the sector selection, Figure , and implements the calculated duty cycle to the appropriate switching vectors. The process provides a base for all the relevant switching states, in all the regions of each sector. No matter where the reference is located within the sector, the duty cycle periods will ensure that the correct states, in the string of possible states, is selected. This is because the regional times calculated, only activate the switching state that corresponds to its duty period, Figure A-14. So each sector is accounted for and all possible switching states are made available. The switch sequencing within each sector ensures that the smallest switching vector is used first and thereafter the medium vectors, followed by the large switching vectors. Also seen in Figure A-14 is the toggling between the upper and lower small switching vectors. This helps with the cancelling of the effect that the small voltage vectors have on the DC bus capacitors.

The output of the duty cycle and switch state processes, in Figure A-13 and Figure A-14, are subsequently sent to the process seen in Figure A-15. Here the gating pulses, for the 3-level NPC converter, are generated and implemented in the model seen in Figure A-9.

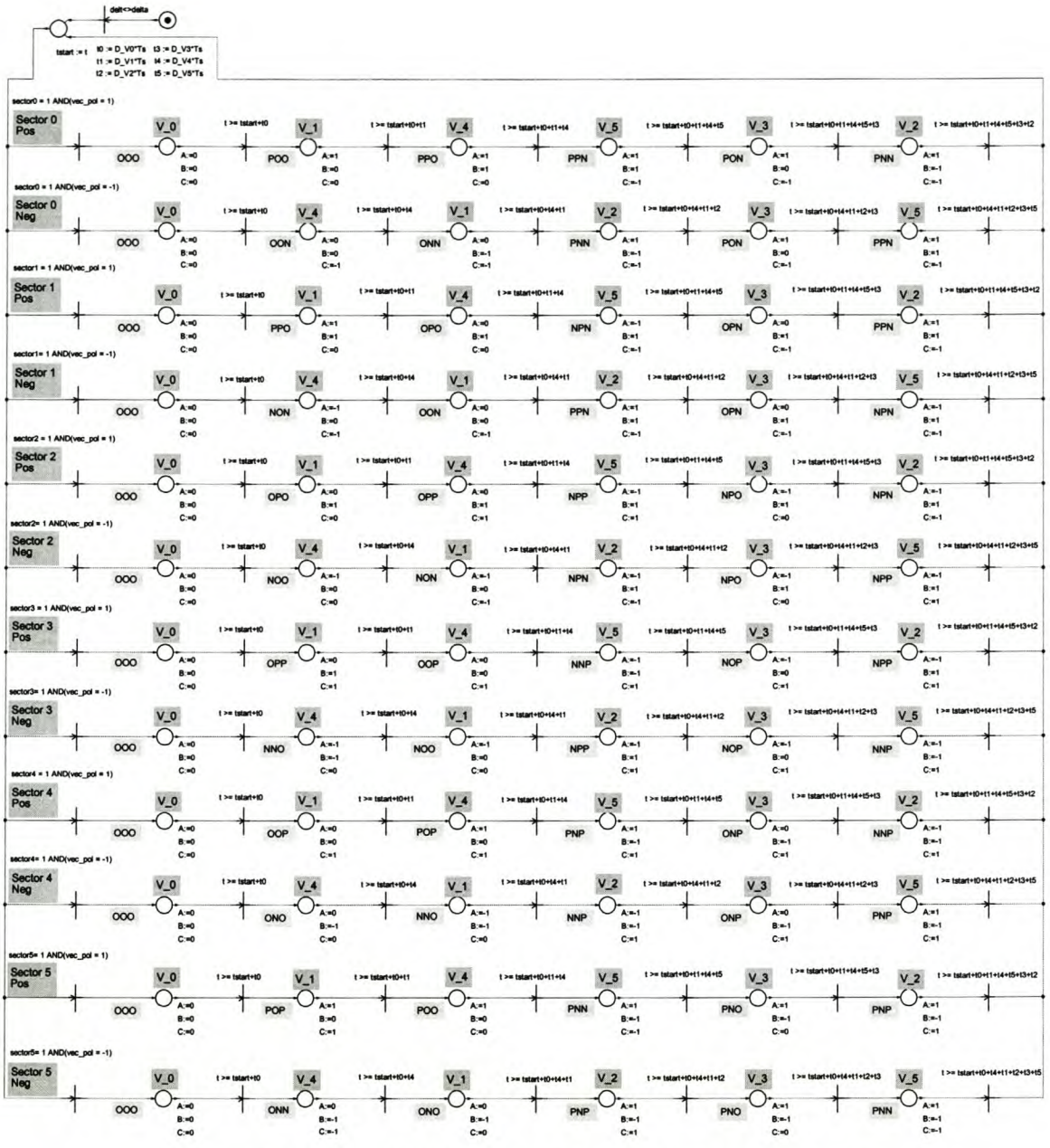


Figure A-14: 3-Level SVM Switching State Determination Process

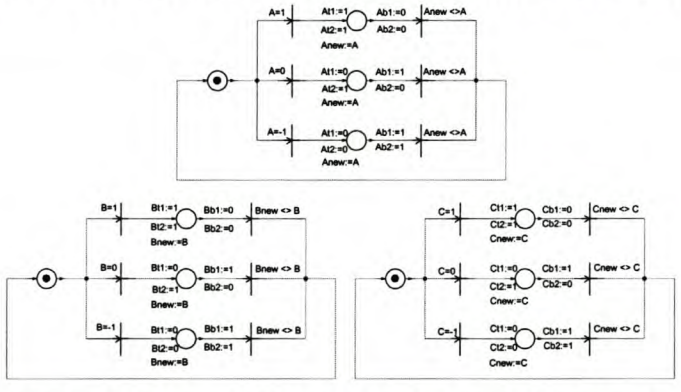


Figure A-15: 3-level SVM gating pulse generation process.

Appendix B Duty Cycle Calculations

B.1 Duty Cycle Calculations for 3-Level SVM for the NPCC

The calculation of the duty cycles for the remaining regions, regions 2 to 4 not covered in Chapter 4, of sector 0 is performed using the same procedure as that for Region 1. The vector placement and duty periods for each vector are seen in Figure B-1, while the vector lengths are seen in Figure B-2.

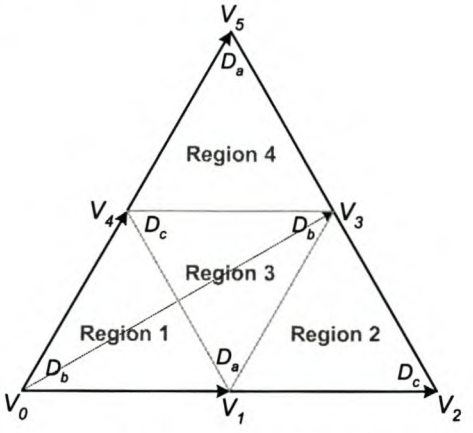


Figure B-1: Vector and Duty Cycle Placement for 3-level SVM

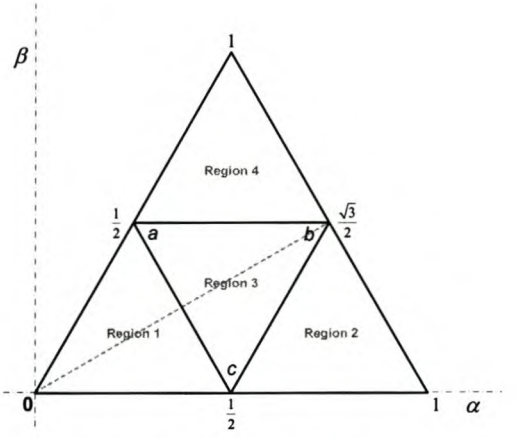


Figure B-2: Vector Lengths

Equation (B.1) is once again used throughout these following calculations as the first assumption.

$$D_a + D_b + D_c = 1 \tag{B.1}$$

Using the vectors in Figure B-1 and the duty ratio makeup of equation (B.1), formulas for all the regions can be derived and are seen below.

Region 2:

$$V_1 \cdot D_a + V_3 \cdot D_b + V_2 \cdot D_c = V_{ref} \tag{B.2}$$

Region 3:

$$V_1 \cdot D_a + V_3 \cdot D_b + V_4 \cdot D_c = V_{ref} \tag{B.3}$$

Region 4:

$$V_5 \cdot D_a + V_3 \cdot D_b + V_4 \cdot D_c = V_{ref} \tag{B.4}$$

Standard trigonometric identities, used extensively in this section, are listed as follows:

$$\begin{aligned} \sin\frac{\pi}{3} &= \frac{\sqrt{3}}{2} \quad AND \quad \sin\frac{\pi}{6} = \frac{1}{2} \\ \cos\frac{\pi}{3} &= \frac{1}{2} \quad AND \quad \cos\frac{\pi}{6} = \frac{\sqrt{3}}{2} \end{aligned} \tag{B.5}$$

Furthermore the definition of the reference vector in its polar format is listed as:

$$r\angle\delta = r\cdot(\cos\delta + j\sin\delta) \tag{B.6}$$

Taken from the Space Vector Modulation theory, the following is also widely used:

$$V_{ref} = V \cdot e^{j\delta} \quad with \quad V = \frac{\sqrt{3}}{2}\cdot m_a \tag{B.7}$$

Using the above identities the duty cycles for each region can be calculated as follows:

B.1.1 Derivation of the Duty Cycle Formulae in Region 2

In this region the vectors shown in (B.2) have the following values, derived from the per unit values seen in Figure B-2.

$$V_1 = \frac{1}{2} \quad AND \quad V_2 = 1 \quad AND \quad V_3 = \frac{\sqrt{3}}{2} \cdot e^{j\frac{\pi}{6}}$$

Using (B.2) and (B.6) the following solution is obtained:

$$\frac{1}{2} \cdot D_a + \frac{\sqrt{3}}{2}\left(\cos\frac{\pi}{6} + j\sin\frac{\pi}{6}\right) \cdot D_b + D_c = V \cdot (\cos\delta + j\sin\delta)$$

These values are then separated into their real and imaginary components. Applying the identities in (B.5) to these real and imaginary values yield the following:

$$\text{Re}: \ \frac{1}{2} \cdot D_a + \frac{3}{4} \cdot D_b + D_c = V\cos\delta \quad AND \quad \text{Im}: \ \frac{\sqrt{3}}{4} \cdot D_b = V\sin\delta$$

Using the above solution and (B.1), a matrix like that seen below is constructed.

$$\begin{bmatrix} 1 & 1 & 1 \\ \frac{1}{2} & \frac{3}{4} & 1 \\ 0 & \frac{\sqrt{3}}{4} & 0 \end{bmatrix} \cdot \begin{bmatrix} D_a \\ D_b \\ D_c \end{bmatrix} = \begin{bmatrix} 1 \\ V\cos\delta \\ V\sin\delta \end{bmatrix}$$

Using Gaussian elimination the following is obtained:

$$\begin{bmatrix} 1 & 1 & 1 \\ 0 & \frac{1}{4} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{4} & 0 \end{bmatrix} \cdot \begin{bmatrix} D_a \\ D_b \\ D_c \end{bmatrix} = \begin{bmatrix} 1 \\ V\cos\delta - \frac{1}{2} \\ V\sin\delta \end{bmatrix} \tag{B.8}$$

Applying the identity (B.7) into (B.8) yields the following for D_b:

$$D_b = 2m_a \cdot \sin\delta \tag{B.9}$$

Substituting (B.9) into the matrix in (B.8), yields the following:

$$\frac{1}{4}D_b + \frac{1}{2}D_c = V \cdot \cos\delta - \frac{1}{2}$$

The equation can be simplified using the identities from (B.5) and yields the following:

$$\begin{aligned} D_c &= V \cdot \left(2\cos\delta - \frac{2}{\sqrt{3}}\sin\delta\right) - 1 \\ &= \frac{4}{\sqrt{3}}V \cdot \left(\frac{\sqrt{3}}{2}\cos\delta - \frac{1}{2}\sin\delta\right) - 1 \\ &= \frac{4}{\sqrt{3}}V \cdot \sin\left(\frac{\pi}{3} - \delta\right) - 1 \end{aligned}$$

Applying (B.7) to this the following is obtained:

$$D_c = 2 \cdot m_a \cdot \sin\left(\frac{\pi}{3} - \delta\right) - 1 \tag{B.10}$$

Substituting (B.10) and (B.9) into the matrix labelled (B.8) enables the solution below to

be obtained. This can be simplified by using identities from (B.5).

$$D_a = 1 - \frac{4}{\sqrt{3}} V \cdot \sin\delta - \frac{4}{\sqrt{3}} V \cdot \left(\frac{\sqrt{3}}{2} \cos\delta - \frac{1}{2} \sin\delta \right) + 1$$

$$\therefore D_a = 2 - \frac{4}{\sqrt{3}} V \cdot \sin\left(\frac{\pi}{3} + \delta \right)$$

Finally using (B.7), the following equation is obtained:

$$D_a = 2 - 2 \cdot m_a \cdot \sin\left(\frac{\pi}{3} + \delta \right) \tag{B.11}$$

A summary of the duty cycle formulae for Region 2 can thus be listed as:

$$D_a = 2 - 2 \cdot m_a \cdot \sin\left(\frac{\pi}{3} + \delta \right)$$

$$D_b = 2 m_a \cdot \sin\delta$$

$$D_c = 2 \cdot m_a \cdot \sin\left(\frac{\pi}{3} - \delta \right) - 1$$

B.1.2 Derivation of the Duty Cycle Formulae in Region 3

In Region 2 the vectors of the equation numbered (B.3) will have the following values, derived from Figure B-2.

$$V_1 = \frac{1}{2} \quad AND \quad V_3 = \frac{\sqrt{3}}{2} \cdot e^{j\frac{\pi}{6}} \quad AND \quad V_4 = \frac{1}{2} \cdot e^{j\frac{\pi}{3}}$$

Using (B.3) and (B.6) the following solution is achieved:

$$\frac{1}{2} \cdot D_a + \frac{\sqrt{3}}{2} \left(\cos\frac{\pi}{6} + j \sin\frac{\pi}{6} \right) \cdot D_b + \frac{1}{2} \left(\cos\frac{\pi}{3} + j \sin\frac{\pi}{3} \right) \cdot D_c = V \cdot \left(\cos\delta + j \sin\delta \right)$$

Separating the real and imaginary components and applying the identities in (B.5) to these real and imaginary values yield the following:

$$\text{Re}: \ \frac{1}{2} \cdot D_a + \frac{3}{4} \cdot D_b + \frac{1}{4} \cdot D_c = V \cos\delta \quad AND \quad \text{Im}: \ \frac{\sqrt{3}}{4} \cdot D_b + \frac{\sqrt{3}}{4} \cdot D_c = V \sin\delta$$

Applying the above solution and (B.1) to a matrix yields the following:

$$\begin{bmatrix} 1 & 1 & 1 \\ \frac{1}{2} & \frac{3}{4} & \frac{1}{4} \\ 0 & \frac{\sqrt{3}}{4} & \frac{\sqrt{3}}{4} \end{bmatrix} \cdot \begin{bmatrix} D_a \\ D_b \\ D_c \end{bmatrix} = \begin{bmatrix} 1 \\ V\cos\delta \\ V\sin\delta \end{bmatrix} \tag{B.12}$$

Using the technique of Gaussian elimination the following is obtained:

$$\begin{bmatrix} 1 & 1 & 1 \\ 0 & \frac{1}{4} & -\frac{1}{4} \\ 0 & 0 & \frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} D_a \\ D_b \\ D_c \end{bmatrix} = \begin{bmatrix} 1 \\ V\cos\delta - \frac{1}{2} \\ V\sin\delta - \sqrt{3} \cdot V\cos\delta + \frac{\sqrt{3}}{2} \end{bmatrix} \tag{B.13}$$

Choosing the equation with the least unknowns, the following can be determined for the duty cycle D_c:

$$\begin{aligned} D_c &= \frac{4}{\sqrt{3}}V\cdot\left(\frac{1}{2}\sin\delta-\frac{\sqrt{3}}{2}\cos\delta\right)+1 \\ &= \frac{4}{\sqrt{3}}V\cdot\left(\cos\frac{\pi}{3}\sin\delta-\sin\frac{\pi}{3}\cos\delta\right)+1 \\ &= \frac{4}{\sqrt{3}}V\cdot\sin\left(\delta-\frac{\pi}{3}\right)+1 \end{aligned} \tag{B.14}$$

Applying (B.7) yields:

$$D_c = 2m_a\cdot\sin\left(\delta-\frac{\pi}{3}\right)+1 \tag{B.15}$$

Reapplying it to the matrix in (B.13), it yields the following:

$$\frac{1}{4}D_b+\frac{1}{4}D_c = V\cdot\cos\delta-\frac{1}{2}$$

Using the identities from (B.5) the equation is rewritten into:

$$\frac{1}{4}D_b = V\cdot\cos\delta-\frac{1}{2}+\frac{1}{4}\left(\frac{4}{\sqrt{3}}V\cdot\left(\frac{1}{2}\sin\delta-\frac{\sqrt{3}}{2}\cos\delta\right)+1\right)$$

$$\begin{aligned} \therefore D_b &= \frac{2}{\sqrt{3}}V\cdot\sin\delta+2V\cdot\cos\delta-1 \\ &= \frac{4}{\sqrt{3}}V\cdot\left(\frac{1}{2}\sin\delta+\frac{\sqrt{3}}{2}\cos\delta\right)-1 \\ &= \frac{4}{\sqrt{3}}V\cdot\left(\cos\frac{\pi}{3}\sin\delta+\sin\frac{\pi}{3}\cos\delta\right)-1 \\ &= \frac{4}{\sqrt{3}}V\cdot\sin\left(\delta+\frac{\pi}{3}\right)-1 \end{aligned}$$

Once again applying (B.7) we get the following:

$$D_b = 2\cdot m_a\cdot\sin\left(\delta+\frac{\pi}{3}\right)-1 \tag{B.16}$$

Applying the solutions from (B.15) and (B.16) into the matrix seen in (B.13) enables the solution below to be determined. Simplifying the solution using (B.5) yields:

$$D_a = 1-\frac{4}{\sqrt{3}}V\cdot\left(\frac{1}{2}\sin\delta+\frac{\sqrt{3}}{2}\cos\delta+\frac{1}{2}\sin\delta-\frac{\sqrt{3}}{2}\cos\delta\right)$$

$$\therefore D_a = 1-\frac{4}{\sqrt{3}}V\cdot\sin\delta$$

Finally using (B.7) the following equation is derived:

$$D_a = 1-2\cdot m_a\cdot\sin\delta \tag{B.17}$$

To summarise, the equations for the duty cycle calculations are listed below:

$$D_a = 1-2\cdot m_a\cdot\sin\delta$$

$$D_b = 2\cdot m_a\cdot\sin\left(\delta+\frac{\pi}{3}\right)-1$$

$$D_c = 2m_a\cdot\sin\left(\delta-\frac{\pi}{3}\right)+1$$

B.1.3 Derivation of the Duty Cycle Formulae in Region 4

In Region 4 the vectors of equation (B.4) have the following values, determined on a per unit basis from Figure B-2.

$$V_3 = \frac{\sqrt{3}}{2}\cdot e^{j\frac{\pi}{6}} \quad AND \quad V_4 = \frac{1}{2}\cdot e^{j\frac{\pi}{3}} \quad AND \quad V_5 = 1\cdot e^{j\frac{\pi}{3}}$$

Using (B.4) and (B.6) the following solution is obtained:

$$\left(\cos\frac{\pi}{3}+j\sin\frac{\pi}{3}\right)\cdot D_a+\frac{\sqrt{3}}{2}\left(\cos\frac{\pi}{6}+j\sin\frac{\pi}{6}\right)\cdot D_b+\frac{1}{2}\cdot\left(\cos\frac{\pi}{3}+j\sin\frac{\pi}{3}\right)\cdot D_c = V\cdot(\cos\delta+j\sin\delta)$$

Separating the real and imaginary components and applying the identities in (B.5) to these real and imaginary values yield the following:

$$\text{Re}:\ \frac{1}{2}\cdot D_a+\frac{3}{4}\cdot D_b+\frac{1}{4}\cdot D_c = V\cos\delta \quad AND \quad \text{Im}:\ \frac{\sqrt{3}}{2}\cdot D_a+\frac{\sqrt{3}}{4}\cdot D_b+\frac{\sqrt{3}}{4}\cdot D_c = V\sin\delta$$

Once again the above solution and (B.1) can be represented by the matrix below:

$$\begin{bmatrix} 1 & 1 & 1 \\ \frac{1}{2} & \frac{3}{4} & \frac{1}{4} \\ \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{4} & \frac{\sqrt{3}}{4} \end{bmatrix}\cdot\begin{bmatrix} D_a \\ D_b \\ D_c \end{bmatrix} = \begin{bmatrix} 1 \\ V\cos\delta \\ V\sin\delta \end{bmatrix} \tag{B.18}$$

Rearranging the matrix to make the Gaussian elimination simpler the following matrix is obtained:

$$\begin{bmatrix} 1 & 1 & 1 \\ \frac{1}{4} & \frac{3}{4} & \frac{1}{2} \\ \frac{\sqrt{3}}{4} & \frac{\sqrt{3}}{4} & \frac{\sqrt{3}}{2} \end{bmatrix}\cdot\begin{bmatrix} D_c \\ D_b \\ D_a \end{bmatrix} = \begin{bmatrix} 1 \\ V\cos\delta \\ V\sin\delta \end{bmatrix}$$

Applying the Gaussian elimination technique the following is obtained:

$$\begin{bmatrix} 1 & 1 & 1 \\ 0 & \frac{1}{2} & \frac{1}{4} \\ 0 & 0 & \frac{\sqrt{3}}{4} \end{bmatrix}\cdot\begin{bmatrix} D_c \\ D_b \\ D_a \end{bmatrix} = \begin{bmatrix} 1 \\ V\cos\delta-\frac{1}{4} \\ V\sin\delta-\frac{\sqrt{3}}{4} \end{bmatrix} \tag{B.19}$$

Choosing D_a, the function with the least unknowns, the following is determined:

$$D_a = \frac{4}{\sqrt{3}}V\cdot\sin\delta-1 \tag{B.20}$$

Applying (B.7) yields:

$$D_a = 2m_a\cdot\sin\delta-1 \tag{B.21}$$

Re-substituting it into the matrix in (B.19), yields the following:

$$\frac{1}{2}D_b+\frac{1}{4}D_a = V\cdot\cos\delta-\frac{1}{4}$$

The identities from (B.5) allow the equation to be rewritten as:

$$D_b = \frac{4}{\sqrt{3}} V \cdot \left(\frac{\sqrt{3}}{2} \cos\delta - \frac{1}{2} \sin\delta \right)$$

$$\therefore D_b = \frac{4}{\sqrt{3}} V \cdot \left(\sin\frac{\pi}{3} \cos\delta - \cos\frac{\pi}{3} \sin\delta \right)$$

$$= \frac{4}{\sqrt{3}} V \cdot \sin\left(\frac{\pi}{3} - \delta \right)$$

Once again applying (B.7) we get the following:

$$D_b = 2 \cdot m_a \cdot \sin\left(\frac{\pi}{3} - \delta \right) \tag{B.22}$$

Applying the solutions from (B.21) and (B.22) into the matrix seen in (B.19) yields the solution below. This is further simplified by using the identities from (B.5).

$$D_c = 2 - \frac{4}{\sqrt{3}} V \cdot \left(\frac{\sqrt{3}}{2} \cos\delta + \frac{1}{2} \sin\delta \right)$$

$$\therefore D_c = 2 - \frac{4}{\sqrt{3}} V \cdot \left(\sin\frac{\pi}{3} \cos\delta + \cos\frac{\pi}{3} \sin\delta \right)$$

$$= 2 - \frac{4}{\sqrt{3}} V \cdot \sin\left(\frac{\pi}{3} + \delta \right)$$

Finally using (B.7) the following equation is derived:

$$D_c = 2 - 2 \cdot m_a \cdot \sin\left(\frac{\pi}{3} + \delta \right) \tag{B.23}$$

So in summary the equations used to calculate the duty cycles in region 4 listed below:

$$D_a = 2m_a \cdot \sin\delta - 1$$

$$D_a = 2m_a \cdot \sin\delta - 1$$

$$D_c = 2 - 2 \cdot m_a \cdot \sin\left(\frac{\pi}{3} + \delta \right)$$

These equations, mentioned in chapter 4, are applied to the simulations and practical model of the NPCC in order to facilitate the 3-level SVM control technique.

Appendix C C-Code for PEC31 Controller

C.1 SSC Normal SVM Code

```
/*__[ main.c
]_____________________________________________________________________
____

   SSC Normal SVM Code for PEC31
    - uses PEC31 support libraries  (Libraries written by A.D. le Roux )
    -

    - function
        - perform Normal SVM open-loop conrol
        - demonstrate the DAC8413 support functions

    G.B.Lee
    - 2003

_____________________________________________________________________
_____________*/

#define _C_MAIN

#include <math.h>
#include <float.h>
#include "type.h"
#include "c3x.h"
#include "dac8413.h"
#include "ad7891.h"
#include "pwm.h"
#include "lcd.h"

/*_____________________________________________________________________
_____________*/
/*__global vari-
ables_____________________________________________________________________
__*/

float  theta = 0.0; /* angle of reference vector in A-B plane */
float  delta = 0.0; /* theta referred back to sector 0 */
float  d0,d1,d2;  /*duty cycles for vectors v1, v2 & v3 */
FLOAT dA,dB,dC;  /*duty cycles for each phase */

FLOAT   wt  =   0.0;
FLOAT   Ma  =   0.0;

UINT    bstate;
UINT    fbe = 0;

/*__Switching period & blanking time__*/
#define Ts  (166.67e-6)
#define Td  (5.0e-6)
#define Tf  (20.0e-3)
#define pi  (3.14159265)

  FLOAT calc_d1(FLOAT x)
  {
```

```
    return (Ma*sin(pi*((1.0)/(3.0))-x)) ;  /*use ma and delta to calculate
duty cycle d1*/
  }

  FLOAT calc_d2(FLOAT x)
  {
    return (Ma*sin(x)) ;      /*use ma and delta to calculate duty cycle
d2*/
  }

/*_____________________________________________________________________
_____________*/
void main()
{

    /*__run at 1 wait-state__*/
    *p_c3x_reg_pbc              =   (3<<3) | (1<<5);
    /*__enable instruction cache__*/
    asm("  or  0800h,st");

    /*__ADCs to standby__*/
    *((VUINT*)0x700000) =   (AD7891_CNTRL_STBY)<<20;
    *((VUINT*)0x700001) =   (AD7891_CNTRL_STBY)<<20;
    *((VUINT*)0x700002) =   (AD7891_CNTRL_STBY)<<20;
    *((VUINT*)0x700003) =   (AD7891_CNTRL_STBY)<<20;

    lcd_init();

    /*__startup PEC31 PWM__*/
    /*__trigger watch dog__*/
    pec31_FPGA_reg->wr.WDTimer  =   2;
    /*__init PWM__*/
    _pec31_FPGA_PWM_init( &pec31_FPGA_PWM[0], Ts, Td );
    _pec31_FPGA_PWM_init( &pec31_FPGA_PWM[1], Ts, Td );
    /*__setup timing__*/
    pec31_FPGA_PWM[0].p_reg->wr.compare[0]      =   100;
    pec31_FPGA_PWM[1].p_reg->wr.compare[0]      =   100;
    /*__setup error feedback: 0x1FF=no feedbacks checked!__*/
    /*  0x1FF = unprotected  */
    /*  0x1C0 = protected    */
    pec31_FPGA_PWM[0].p_reg->wr.error_mask      =   0x0103;
    pec31_FPGA_PWM[1].p_reg->wr.error_mask      =   0x0103;
    /*__clear error feedback__*/
    pec31_FPGA_PWM[0].p_reg->rd.error_status;
    pec31_FPGA_PWM[1].p_reg->rd.error_status;
    /*__set all duty cycles to 50% and enable PWM__*/
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 0, 0.5 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 1, 0.5 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 2, 0.5 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 3, 0.5 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 0, 0.5 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 1, 0.5 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 2, 0.5 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 3, 0.5 );
    pec31_FPGA_reg->wr.PWM_control      =   0x33;

    while (1)
    {
        /*__update reference phase__*/
        theta   +=  ((Ts)/(Tf))*2.0*3.1416;
        theta   +=  ( theta<2.0*pi ? 0.0 : -2.0*3.1416 );
```

```
        /*__check push buttons__*/
        bstate  =   pec31_FPGA_reg->rd.Din;
        if ((bstate&0x20)!=0)
        {
            Ma      -=  100.0e-3*Ts;
        }
        else
        {
            if ((bstate&0x10)!=0)
            {
                Ma      +=  50.0e-3*Ts;
            }
        }
        Ma      =   ( Ma<0.0 ? 0.0 : Ma );
        Ma      =   ( Ma>1.0 ? 1.0 : Ma );


        /*__turn on LED__*/
        *((VUINT*)0x700023) =   0x01;

        /*__poll for end of PWM cycle__*/
        while ((pec31_FPGA_reg->rd.PWM_status & 0x01) != 0);
        while ((pec31_FPGA_reg->rd.PWM_status & 0x01) == 0);

        /*__turn off LED__*/
        *((VUINT*)0x700023) =   0x00;

if (theta<((1.0)/(3.0))*pi)    /* sector 0 */
        {
  delta = theta;
  d1 = calc_d1(delta);
  d2 = calc_d2(delta);
  d0 = (1.0-d1-d2)*(0.5);

  dC = d0;
  dB = (d0+d2);
  dA = (d0+d2+d1);
}

else if (theta<((2.0)/(3.0))*pi) /* sector 1 */
        {
  delta = theta-((1.0)/(3.0))*pi;
  d1 = calc_d1(delta);
  d2 = calc_d2(delta);
  d0 = (1.0-d1-d2)*(0.5);

  dC = d0;
  dB = (d0+d1+d2);
  dA = (d0+d1);
}

else if (theta<pi)      /* sector 2 */
        {
  delta = theta-((2.0)/(3.0))*pi;
  d1 = calc_d1(delta);
  d2 = calc_d2(delta);
  d0 = (1.0-d1-d2)*(0.5);

  dC = (d0+d2);
  dB = (d0+d2+d1);
```

```
  dA = d0;
}

else if (theta<((4.0)/(3.0))*pi) /* sector 3 */
      {
  delta = theta-pi;
  d1 = calc_d1(delta);
  d2 = calc_d2(delta);
  d0 = (1.0-d1-d2)*(0.5);

  dC = (d0+d1+d2);
  dB = (d0+d1);
  dA = d0;
}

else if (theta<((5.0)/(3.0))*pi) /* sector 4 */
      {
  delta = theta-((4.0)/(3.0))*pi;
  d1 = calc_d1(delta);
  d2 = calc_d2(delta);
  d0 = (1.0-d1-d2)*(0.5);

  dC = (d0+d2+d1);
  dB = d0;
  dA = (d0+d2);
}

else if (theta<(2.0*pi))     /* sector 5 */
      {
  delta = theta-((5.0)/(3.0))*pi;
  d1 = calc_d1(delta);
  d2 = calc_d2(delta);
  d0 = (1.0-d1-d2)*(0.5);

  dC = (d0+d1);
  dB = d0;
  dA = (d0+d1+d2);
}

      /*__update FPGA PWM registers__*/
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 0, dA );
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 1, dB );
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 2, dC );
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 0, dA );
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 1, dB );
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 2, dC );


      /*__write current phase & duty cycles to the DAC__*/
      _dac8413_update_v( &pec31_dac8413, 0, Ma );
      _dac8413_update_v( &pec31_dac8413, 1, dA );
      _dac8413_update_v( &pec31_dac8413, 2, dB );
      _dac8413_update_v( &pec31_dac8413, 3, dC );


      fbe = (fbe | pec31_FPGA_PWM[0].p_reg->rd.error_status) & 0x1FF;
      fbe = (fbe | pec31_FPGA_PWM[1].p_reg->rd.error_status) & 0x1FF;


      lcd_goto(0,0);
      lcd_prints_ex("Ma   = ");
```

```
        lcd_printi_ex(100.0*Ma,6,TRUE);
        lcd_fill_ex(' ');
        lcd_goto(0,1);
        lcd_prints_ex("FBE = ");
        lcd_printi_ex(fbe,6,TRUE);
        lcd_fill_ex(' ');
        lcd_ex();


        /*__trigger the dog__*/
        if (fbe == 0)
  {
    pec31_FPGA_reg->wr.WDTimer  =   2;
  }


    }

}
```

C.2 SSC Interleaved SVM Code

```
/*__[ main.c
]_____________________________________________________________________
____

      SSC Normal SVM Code for PEC31
    - uses PEC31 support libraries  (Libraries written by A.D. le Roux )
    -

    - function
        - perform Normal SVM open-loop conrol
        - demonstrate the DAC8413 support functions

    G.B.Lee
    - 2003

_____________________________________________________________________
_____________*/

#define _C_MAIN
#include <math.h>
#include <float.h>
#include "type.h"
#include "c3x.h"
#include "dac8413.h"
#include "ad7891.h"
#include "pwm.h"
#include "lcd.h"



/*_____________________________________________________________________
_____________*/
/*__global vari-
ables_____________________________________________________________________
__*/

float  theta = 0.0; /* angle of reference vector in A-B plane */
```

```
float  delta = 0.0; /* theta referred back to sector 0 */
float  d0,d1,d2;  /*duty cycles for vectors v1, v2 & v3 */
FLOAT dA,dB,dC;  /*duty cycles for each phase */

FLOAT   wt  =   0.0;
FLOAT   Ma  =   0.0;



UINT    bstate;
UINT    fbe = 0;

INT polarity = 1;  /*used to toggle duty-cycle writing between PWM0 & PWM1
*/

/*__Switching period & blanking time__*/
#define Ts  (166.67e-6)
#define Td  (5.0e-6)
#define Tf  (20.0e-3)
#define pi  (3.14159265)

  FLOAT calc_d1(FLOAT x)
  {
    return (Ma*sin(pi*((1.0)/(3.0))-x)) ;  /*use ma and delta to calculate
duty cycle d1*/
  }

  FLOAT calc_d2(FLOAT x)
  {
    return (Ma*sin(x)) ;      /*use ma and delta to calculate duty cycle
d2*/
  }


/*_____________________________________________________________________
_____________*/
void main()
{

    /*__run at 1 wait-state__*/
    *p_c3x_reg_pbc              =   (3<<3) | (1<<5);
    /*__enable instruction cache__*/
    asm("  or  0800h,st");

    /*__ADCs to standby__*/
    *((VUINT*)0x700000) =   (AD7891_CNTRL_STBY)<<20;
    *((VUINT*)0x700001) =   (AD7891_CNTRL_STBY)<<20;
    *((VUINT*)0x700002) =   (AD7891_CNTRL_STBY)<<20;
    *((VUINT*)0x700003) =   (AD7891_CNTRL_STBY)<<20;

    lcd_init();

    /*__startup PEC31 PWM__*/
    /*__trigger watch dog__*/
    pec31_FPGA_reg->wr.WDTimer  =   2;
    /*__init PWM__*/
    _pec31_FPGA_PWM_init( &pec31_FPGA_PWM[0], Ts, Td );
    _pec31_FPGA_PWM_init( &pec31_FPGA_PWM[1], Ts, Td );

/*__setup timing__*/
```

```
    pec31_FPGA_PWM[0].p_reg->wr.compare[1]      =
pec31_FPGA_PWM[0].count_max;
    pec31_FPGA_PWM[1].p_reg->wr.compare[0]      =   100;

/*was this:
    pec31_FPGA_PWM[0].p_reg->wr.compare[0]      =   100;
    pec31_FPGA_PWM[1].p_reg->wr.compare[0]      =   100;*/

    /*__setup error feedback: 0x1FF=no feedbacks checked!__*/
    /*  0x1FF = unprotected  */
    /*  0x1C0 = protected    */
    pec31_FPGA_PWM[0].p_reg->wr.error_mask      =   0x0103;
    pec31_FPGA_PWM[1].p_reg->wr.error_mask      =   0x0103;
    /*__clear error feedback__*/
    pec31_FPGA_PWM[0].p_reg->rd.error_status;
    pec31_FPGA_PWM[1].p_reg->rd.error_status;
    /*__set all duty cycles to 50% and enable PWM__*/
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 0, 0.5 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 1, 0.5 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 2, 0.5 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 3, 0.5 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 0, 0.5 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 1, 0.5 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 2, 0.5 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 3, 0.5 );
    pec31_FPGA_reg->wr.PWM_control      =   0x73;


    while (1)
    {
        /*__update reference phase__*/
        theta   +=  ((Ts)/(Tf))*2.0*3.1416*0.5;   /*dividing by 2 again to
let cycle run twice as fast FOR INTERLEAVING */
        theta   +=  ( theta<2.0*pi ? 0.0 : -2.0*3.1416 );

        /*__check push buttons__*/
        bstate  =   pec31_FPGA_reg->rd.Din;
        if ((bstate&0x20)!=0)
        {
            Ma      -=  100.0e-3*Ts;
        }
        else
        {
            if ((bstate&0x10)!=0)
            {
                Ma      +=  50.0e-3*Ts;
            }
        }
        Ma      =   ( Ma<0.0 ? 0.0 : Ma );
        Ma      =   ( Ma>1.0 ? 1.0 : Ma );


        /*__turn on LED__*/
        *((VUINT*)0x700023) =   0x01;

        /*__poll for end of PWM cycle__*/

        if (polarity == 1)      /* done only once per PWM period */
          /* - routine is running at twice switching frequency */
     {
    while ((pec31_FPGA_reg->rd.PWM_status & 0x01) != 0);
```

```
        while ((pec31_FPGA_reg->rd.PWM_status & 0x01) == 0);
      }

       /*__turn off LED__*/
       *((VUINT*)0x700023) =   0x00;


if (theta<((1.0)/(3.0))*pi)    /* sector 0 */
      {
  delta = theta;
  d1 = calc_d1(delta);
  d2 = calc_d2(delta);
  d0 = (1.0-d1-d2)*(0.5);

  dC = d0;
  dB = (d0+d2);
  dA = (d0+d2+d1);
}

else if (theta<((2.0)/(3.0))*pi) /* sector 1 */
      {
  delta = theta-((1.0)/(3.0))*pi;
  d1 = calc_d1(delta);
  d2 = calc_d2(delta);
  d0 = (1.0-d1-d2)*(0.5);

  dC = d0;
  dB = (d0+d1+d2);
  dA = (d0+d1);
}

else if (theta<pi)      /* sector 2 */
      {
  delta = theta-((2.0)/(3.0))*pi;
  d1 = calc_d1(delta);
  d2 = calc_d2(delta);
  d0 = (1.0-d1-d2)*(0.5);

  dC = (d0+d2);
  dB = (d0+d2+d1);
  dA = d0;
}

else if (theta<((4.0)/(3.0))*pi) /* sector 3 */
      {
  delta = theta-pi;
  d1 = calc_d1(delta);
  d2 = calc_d2(delta);
  d0 = (1.0-d1-d2)*(0.5);

  dC = (d0+d1+d2);
  dB = (d0+d1);
  dA = d0;
}

else if (theta<((5.0)/(3.0))*pi) /* sector 4 */
      {
  delta = theta-((4.0)/(3.0))*pi;
  d1 = calc_d1(delta);
  d2 = calc_d2(delta);
  d0 = (1.0-d1-d2)*(0.5);
```

```
  dC = (d0+d2+d1);
  dB = d0;
  dA = (d0+d2);
}

else if (theta<(2.0*pi))      /* sector 5 */
      {
  delta = theta-((5.0)/(3.0))*pi;
  d1 = calc_d1(delta);
  d2 = calc_d2(delta);
  d0 = (1.0-d1-d2)*(0.5);

  dC = (d0+d1);
  dB = d0;
  dA = (d0+d1+d2);
}


      /*__update FPGA PWM registers__*/

if (polarity == -1)
  {
  _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 0, dA );
        _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 1, dB );
        _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 2, dC );
  }

if (polarity == 1)
  {
        _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 0, dA );
        _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 1, dB );
        _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 2, dC );
  }

/*testing phase shift*/

/*_pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 0, 0.5 );
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 1, 0.5 );
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 2, 0.5 );
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 0, 0.5 );
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 1, 0.5 );
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 2, 0.5 );*/


      /*__write current phase & duty cycles to the DAC__*/
      _dac8413_update_v( &pec31_dac8413, 0, Ma );
      _dac8413_update_v( &pec31_dac8413, 1, dA );
      _dac8413_update_v( &pec31_dac8413, 2, dB );
      _dac8413_update_v( &pec31_dac8413, 3, dC );

      fbe = (fbe | pec31_FPGA_PWM[0].p_reg->rd.error_status) & 0x1FF;
      fbe = (fbe | pec31_FPGA_PWM[1].p_reg->rd.error_status) & 0x1FF;

      lcd_goto(0,0);
      lcd_prints_ex("Ma  = ");
      lcd_printi_ex(100.0*Ma,6,TRUE);
      lcd_fill_ex(' ');
      lcd_goto(0,1);
      lcd_prints_ex("FBE = ");
      lcd_printi_ex(fbe,6,TRUE);
```

```
        lcd_fill_ex(' ');
        lcd_ex();

  /*__trigger the dog__*/
        if (fbe == 0)
  {
    pec31_FPGA_reg->wr.WDTimer  =   2;
  }


  polarity *= -1;

    }

}
```

C.3 NPCC 3-level SVM Code

```
/*-----------------Started 02/08/2001----------------
 *
 /*__[ main.c
]_____________________________________________________________
____

      NPCC 3-level SVM Code for PEC31
    - uses PEC31 support libraries  (Libraries written by A.D. le Roux )
    -

    - function
        - perform Normal SVM open-loop conrol
        - demonstrate the DAC8413 support functions

    G.B.Lee
    - 2003
 * ------------------------------------------------*/

#define _C_MAIN

#include <math.h>
#include <float.h>
#include "type.h"
#include "c3x.h"
#include "pwm.h"
#include "dac8413.h"
#include "ad7891.h"
#include "lcd.h"

/*-------------------------------------------------
 * Global Variables
 * ------------------------------------------------*/

INT  TC = 0;

FLOAT theta = 0.0;                    /* phase of reference vector */
FLOAT ma = 0.4;                      /* modulation index */
FLOAT Da,Db,Dc;                      /* duty cycle vectors */
UINT v1,v2,v3;                       /* three vectors to switch */
FLOAT sD1,sD2,sD3;                   /* correct duty cycles for each
vector */
```

```
FLOAT delta;                            /* equivalent to theta but
0&ltdelta<(pi/3) */
INT reg;                                /* region which reference vector is
in */
INT posV = 1;                           /* use + vectors else (posV=0) use
- vectors */
INT ripple = 0;                         /* counter for 150Hz ripple */
INT rippleEn = 0;                       /* ripple enable 0 = off 1 = on */

UINT bstate;                            /* button state */
UINT    fbe = 0;


#define Ts (166.6667e-6)                /* sampling period */
#define Td (5e-6)                       /* dead time */
#define Tf (20e-3)                      /* fundemental frequency */
#define pi (3.14159265359)              /* pi */
#define ma_m (200e-3)      /* ma multiplier for buttons */

/*----------------Vector Definitions----------------
 * Each vector code is 6 bits long
 * Each pair of bits represents the state of one phase
 * 00 = zero
 * 01 = positive
 * 10 = negative
 *
 * e.g. 000110 = 0x06
 *      A = zero
 *      B = positive
 *      C = negative
 *
 * ------------------------------------------------*/
#define OOO (0x00)                  /* zero vector            000000 */
#define POO (0x10)                  /* positive small vector  010000 */
#define ONN (0x0A)                  /* negaitive small vector 001010 */
#define PPO (0x14)                  /* positive small vector  010100 */
#define OON (0x02)                  /* negaitive small vector 000010 */
#define OPO (0x04)                  /* positive small vector  000100 */
#define NON (0x22)                  /* negaitive small vector 100010 */
#define OPP (0x05)                  /* positive small vector  000101 */
#define NOO (0x20)                  /* negaitive small vector 100000 */
#define OOP (0x01)                  /* positive small vector  000001 */
#define NNO (0x28)                  /* negaitive small vector 101000 */
#define POP (0x11)                  /* positive small vector  010001 */
#define ONO (0x08)                  /* negaitive small vector 001000 */
#define PON (0x12)                  /* medium vector          010010 */
#define OPN (0x06)                  /* medium vector          000110 */
#define NPO (0x24)                  /* medium vector          100100 */
#define NOP (0x21)                  /* medium vector          100001 */
#define ONP (0x09)                  /* medium vector          001001 */
#define PNO (0x18)                  /* medium vector          011000 */
#define PNN (0x1A)                  /* large vector           011010 */
#define PPN (0x16)                  /* large vector           010110 */
#define NPN (0x26)                  /* large vector           100110 */
#define NPP (0x25)                  /* large vector           100101 */
#define NNP (0x29)                  /* large vector           101001 */
#define PNP (0x19)                  /* large vector           011001 */

/*-------------------------------------------------
 *
 * Main code body
```

```
 *
 * ------------------------------------------------*/

void main() {


    /* Run at 1 wait-state */
    *p_c3x_reg_pbc              =   (3<<3) | (1<<5);
    /* Enable instruction cache */
    asm("  or  0800h,st");

    lcd_init();


    /* Trigger watch dog */

     pec31_FPGA_reg->wr.WDTimer  =   2;

    *((volatile unsigned int*)0x7000b0) = 0xFFF;

    /* Set all vectors to zero */
    _pec31_FPGA_PWM_vector( &pec31_FPGA_PWM[0], 0, 0 );
    _pec31_FPGA_PWM_vector( &pec31_FPGA_PWM[0], 1, 0 );
    _pec31_FPGA_PWM_vector( &pec31_FPGA_PWM[0], 2, 0 );
    _pec31_FPGA_PWM_vtimes( &pec31_FPGA_PWM[1], 0, 0.2 );
    _pec31_FPGA_PWM_vtimes( &pec31_FPGA_PWM[1], 1, 0.3 );
    _pec31_FPGA_PWM_vtimes( &pec31_FPGA_PWM[1], 2, 0.5 );

    pec31_FPGA_reg->wr.PWM_control      =   0x33;



    while (1) {

        /* Adjust modulation index with push buttons */


  /*bstate  =   pec31_FPGA_reg->rd.Din;*/

        bstate  =   *((volatile unsigned int*)0x70008f);

  if ((bstate&0x20)!=0)
        {
                ma  -=  100.0e-6*ma_m;          /* decrease duty cycle */
        }
        else
        {
            if ((bstate&0x10)!=0)
            {
                ma  +=  50.0e-6*ma_m;          /* increase duty cycle */
            }
        }
        ma  =  ( ma<0.0 ? 0.0 : ma );
        ma  =  ( ma>1.0 ? 1.0 : ma );

        /* Turn on LED */
        *((VUINT*)0x700023) =   0x01;

        /* Poll for end of PWM cycle */
        /* Uses compares (see manual) to check for end of triangle */
        while ((pec31_FPGA_reg->rd.PWM_status & 0x06) != 0);
```

```
        while ((pec31_FPGA_reg->rd.PWM_status & 0x06) == 0);

        /*  Turn off LED */
        *((VUINT*)0x700023) =   0x00;

        /*-----------------------------------------------------
         * Determine duty cycles
         * -----------------------------------------------------*/

        /* Determine delta */
        delta = theta;
        while (delta>(1.0/3.0)*pi) {
            delta -= (1.0/3.0)*pi;                  /* clamp delta to < 60
degrees */
        }

        if ( 2*ma*sin(pi/3+delta) <= 1 ) {           /* Region 1 */
            reg = 1;
            Da = 2*ma*sin(pi/3-delta);
            Db = 1-2*ma*sin(pi/3+delta);
            Dc = 2*ma*sin(delta);
        } else if ( 2*ma*sin(pi/3-delta) >= 1 ) {    /* Region 2 */
            reg = 2;
            Da = 2-2*ma*sin(pi/3+delta);
            Db = 2*ma*sin(delta);
            Dc = 2*ma*sin(pi/3-delta)-1;
        } else if ( 2*ma*sin(delta) >= 1 ) {         /* Region 4 */
            reg = 4;
            Da = 2*ma*sin(delta)-1;
            Db = 2*ma*sin(pi/3-delta);
            Dc = 2-2*ma*sin(pi/3+delta);
        } else {                                     /* Region 3 */
            reg = 3;
            Da = 1-2*ma*sin(delta);
            Db = 2*ma*sin(delta+pi/3)-1;
            Dc = 2*ma*sin(delta-pi/3)+1;
        }

        /*-----------------------------------------------------
         * Determine which sector reference vector is in
         * and determine switches duty cycles
         * -----------------------------------------------------*/
        if ( theta < (1.0/3.0)*pi ) {              /* Sector 0 */
            if ( posV == 1 ) {
                if ( reg == 1 ) {
                    v1 = OOO;
                    v2 = POO;
                    v3 = PPO;
                    sD1 = Db;
                    sD2 = Da;
                    sD3 = Dc;
                } else if ( reg == 2 ) {
                    v1 = POO;
                    v2 = PNN;
                    v3 = PON;
                    sD1 = Da;
                    sD2 = Dc;
                    sD3 = Db;
                } else if ( reg == 3 ) {
                    v1 = POO;
                    v2 = PPO;
```

```
            v3 = PON;
            sD1 = Da;
            sD2 = Dc;
            sD3 = Db;
        } else if ( reg == 4 ) {
            v1 = PPO;
            v2 = PON;
            v3 = PPN;
            sD1 = Dc;
            sD2 = Db;
            sD3 = Da;
        }
    } else {
        if ( reg == 1 ) {
            v1 = OOO;
            v2 = ONN;
            v3 = OON;
            sD1 = Db;
            sD2 = Da;
            sD3 = Dc;
        } else if ( reg == 2) {
            v1 = ONN;
            v2 = PNN;
            v3 = PON;
            sD1 = Da;
            sD2 = Dc;
            sD3 = Db;
        } else if ( reg == 3 ) {
            v1 = ONN;
            v2 = OON;
            v3 = PON;
            sD1 = Da;
            sD2 = Dc;
            sD3 = Db;
        } else if ( reg == 4 ) {
            v1 = OON;
            v2 = PON;
            v3 = PPN;
            sD1 = Dc;
            sD2 = Db;
            sD3 = Da;
        }
    }
} else if ( theta < (2.0/3.0)*pi ) {      /* Sector 1 */
    if ( posV == 1 ) {
        if ( reg == 1 ) {
            v1 = OOO;
            v2 = PPO;
            v3 = OPO;
            sD1 = Db;
            sD2 = Da;
            sD3 = Dc;
        } else if ( reg == 2 ) {
            v1 = PPO;
            v2 = PPN;
            v3 = OPN;
            sD1 = Da;
            sD2 = Dc;
            sD3 = Db;
        } else if ( reg == 3 ) {
            v1 = PPO;
```

```
            v2 = OPO;
            v3 = OPN;
            sD1 = Da;
            sD2 = Dc;
            sD3 = Db;
        } else if ( reg == 4 ) {
            v1 = OPO;
            v2 = OPN;
            v3 = NPN;
            sD1 = Dc;
            sD2 = Db;
            sD3 = Da;
        }
    } else {
        if ( reg == 1 ) {
            v1 = OOO;
            v2 = OON;
            v3 = NON;
            sD1 = Db;
            sD2 = Da;
            sD3 = Dc;
        } else if ( reg == 2) {
            v1 = OON;
            v2 = PPN;
            v3 = OPN;
            sD1 = Da;
            sD2 = Dc;
            sD3 = Db;
        } else if ( reg == 3 ) {
            v1 = OON;
            v2 = NON;
            v3 = OPN;
            sD1 = Da;
            sD2 = Dc;
            sD3 = Db;
        } else if ( reg == 4 ) {
            v1 = NON;
            v2 = OPN;
            v3 = NPN;
            sD1 = Dc;
            sD2 = Db;
            sD3 = Da;
        }
    }
} else if ( theta < pi ) {                    /* Sector 2 */
    if ( posV == 1 ) {
        if ( reg == 1 ) {
            v1 = OOO;
            v2 = OPO;
            v3 = OPP;
            sD1 = Db;
            sD2 = Da;
            sD3 = Dc;
        } else if ( reg == 2 ) {
            v1 = OPO;
            v2 = NPN;
            v3 = NPO;
            sD1 = Da;
            sD2 = Dc;
            sD3 = Db;
        } else if ( reg == 3 ) {
```

```
            v1 = OPO;
            v2 = OPP;
            v3 = NPO;
            sD1 = Da;
            sD2 = Dc;
            sD3 = Db;
        } else if ( reg == 4 ) {
            v1 = OPP;
            v2 = NPO;
            v3 = NPP;
            sD1 = Dc;
            sD2 = Db;
            sD3 = Da;
        }
    } else {
        if ( reg == 1 ) {
            v1 = OOO;
            v2 = NON;
            v3 = NOO;
            sD1 = Db;
            sD2 = Da;
            sD3 = Dc;
        } else if ( reg == 2) {
            v1 = NON;
            v2 = NPN;
            v3 = NPO;
            sD1 = Da;
            sD2 = Dc;
            sD3 = Db;
        } else if ( reg == 3 ) {
            v1 = NON;
            v2 = NOO;
            v3 = NPO;
            sD1 = Da;
            sD2 = Dc;
            sD3 = Db;
        } else if ( reg == 4 ) {
            v1 = NOO;
            v2 = NPO;
            v3 = NPP;
            sD1 = Dc;
            sD2 = Db;
            sD3 = Da;
        }
    }
} else if ( theta < (4.0/3.0)*pi ) {       /* Sector 3 */
    if ( posV == 1 ) {
        if ( reg == 1 ) {
            v1 = OOO;
            v2 = OPP;
            v3 = OOP;
            sD1 = Db;
            sD2 = Da;
            sD3 = Dc;
        } else if ( reg == 2 ) {
            v1 = OPP;
            v2 = NPP;
            v3 = NOP;
            sD1 = Da;
            sD2 = Dc;
            sD3 = Db;
```

```
            } else if ( reg == 3 ) {
                v1 = OPP;
                v2 = OOP;
                v3 = NOP;
                sD1 = Da;
                sD2 = Dc;
                sD3 = Db;
            } else if ( reg == 4 ) {
                v1 = OOP;
                v2 = NOP;
                v3 = NNP;
                sD1 = Dc;
                sD2 = Db;
                sD3 = Da;
            }
        } else {
            if ( reg == 1 ) {
                v1 = OOO;
                v2 = NOO;
                v3 = NNO;
                sD1 = Db;
                sD2 = Da;
                sD3 = Dc;
            } else if ( reg == 2) {
                v1 = NOO;
                v2 = NPP;
                v3 = NOP;
                sD1 = Da;
                sD2 = Dc;
                sD3 = Db;
            } else if ( reg == 3 ) {
                v1 = NOO;
                v2 = NNO;
                v3 = NOP;
                sD1 = Da;
                sD2 = Dc;
                sD3 = Db;
            } else if ( reg == 4 ) {
                v1 = NNO;
                v2 = NOP;
                v3 = NNP;
                sD1 = Dc;
                sD2 = Db;
                sD3 = Da;
            }
        }
    } else if ( theta < (5.0/3.0)*pi ) {       /* Sector 4 */
        if ( posV == 1 ) {
            if ( reg == 1 ) {
                v1 = OOO;
                v2 = OOP;
                v3 = POP;
                sD1 = Db;
                sD2 = Da;
                sD3 = Dc;
            } else if ( reg == 2 ) {
                v1 = OOP;
                v2 = NNP;
                v3 = ONP;
                sD1 = Da;
                sD2 = Dc;
```

```
            sD3 = Db;
        } else if ( reg == 3 ) {
            v1 = OOP;
            v2 = POP;
            v3 = ONP;
            sD1 = Da;
            sD2 = Dc;
            sD3 = Db;
        } else if ( reg == 4 ) {
            v1 = POP;
            v2 = ONP;
            v3 = PNP;
            sD1 = Dc;
            sD2 = Db;
            sD3 = Da;
        }
    } else {
        if ( reg == 1 ) {
            v1 = OOO;
            v2 = NNO;
            v3 = ONO;
            sD1 = Db;
            sD2 = Da;
            sD3 = Dc;
        } else if ( reg == 2) {
            v1 = NNO;
            v2 = NNP;
            v3 = ONP;
            sD1 = Da;
            sD2 = Dc;
            sD3 = Db;
        } else if ( reg == 3 ) {
            v1 = NNO;
            v2 = ONO;
            v3 = ONP;
            sD1 = Da;
            sD2 = Dc;
            sD3 = Db;
        } else if ( reg == 4 ) {
            v1 = ONO;
            v2 = ONP;
            v3 = PNP;
            sD1 = Dc;
            sD2 = Db;
            sD3 = Da;
        }
    }
} else {                                    /* Sector 5 */
    if ( posV == 1 ) {
        if ( reg == 1 ) {
            v1 = OOO;
            v2 = POP;
            v3 = POO;
            sD1 = Db;
            sD2 = Da;
            sD3 = Dc;
        } else if ( reg == 2 ) {
            v1 = POP;
            v2 = PNP;
            v3 = PNO;
            sD1 = Da;
```

```
            sD2 = Dc;
            sD3 = Db;
        } else if ( reg == 3 ) {
            v1 = POP;
            v2 = POO;
            v3 = PNO;
            sD1 = Da;
            sD2 = Dc;
            sD3 = Db;
        } else if ( reg == 4 ) {
            v1 = POO;
            v2 = PNO;
            v3 = PNN;
            sD1 = Dc;
            sD2 = Db;
            sD3 = Da;
        }
    } else {
        if ( reg == 1 ) {
            v1 = OOO;
            v2 = ONO;
            v3 = ONN;
            sD1 = Db;
            sD2 = Da;
            sD3 = Dc;
        } else if ( reg == 2) {
            v1 = ONO;
            v2 = PNP;
            v3 = PNO;
            sD1 = Da;
            sD2 = Dc;
            sD3 = Db;
        } else if ( reg == 3 ) {
            v1 = ONO;
            v2 = ONN;
            v3 = PNO;
            sD1 = Da;
            sD2 = Dc;
            sD3 = Db;
        } else if ( reg == 4 ) {
            v1 = ONN;
            v2 = PNO;
            v3 = PNN;
            sD1 = Dc;
            sD2 = Db;
            sD3 = Da;
        }
    }
}

/* Write duty cycles to PWM output */
_pec31_FPGA_PWM_vector( &pec31_FPGA_PWM[0], 0, v1 );
_pec31_FPGA_PWM_vector( &pec31_FPGA_PWM[0], 1, v2 );
_pec31_FPGA_PWM_vector( &pec31_FPGA_PWM[0], 2, v3 );
_pec31_FPGA_PWM_vtimes( &pec31_FPGA_PWM[1], 0, sD1 );
_pec31_FPGA_PWM_vtimes( &pec31_FPGA_PWM[1], 1, sD2 );
_pec31_FPGA_PWM_vtimes( &pec31_FPGA_PWM[1], 2, sD3 );


/* Output duty cycles to DAC for testing */
```

```
        _dac8413_update_v( &pec31_dac8413, 0, 10*sD1 );     /* Positive
state duty cycle */
        _dac8413_update_v( &pec31_dac8413, 1, 10*sD2 );   /* Zero state
duty cycle */
        _dac8413_update_v( &pec31_dac8413, 2, 10*sD3 );     /* Negative
state duty cycle */
        _dac8413_update_v( &pec31_dac8413, 3, 10*ma );


        /* Rotate reference vector */
        theta += ((Ts)/(Tf))*2.0*pi;
        theta += ( theta<(2.0*pi) ? 0.0 : -2.0*pi);

        /* Invert PosV */
        posV += ( posV < 1.0 ? 1.0 : -1.0);


        /*fbe = (fbe | pec31_FPGA_PWM[0].p_reg->rd.error_status) & 0x1FF;
        fbe = (fbe | pec31_FPGA_PWM[1].p_reg->rd.error_status) & 0x1FF;  */

        fbe = (fbe | *((volatile unsigned int*)0x7000b0)) & 0xFFF;


        lcd_goto(0,0);
        lcd_prints_ex("Ma  = ");
        lcd_printi_ex(100.0*ma,6,TRUE);
        lcd_fill_ex(' ');
        lcd_goto(0,1);
        lcd_prints_ex("FBE = ");
        lcd_printi_ex(fbe,6,TRUE);
        lcd_fill_ex(' ');
        lcd_ex();

  /*test to allow watchcdog to time out*/

  /*
  if((bstate&amp0x10)!=0)
    {
     while (1);
    }
  */


        /*__trigger the dog__*/
        if (fbe == 0)
  {
    pec31_FPGA_reg->wr.WDTimer  =   2;
  }


    }
}
```

Appendix D Modified FPGA Routine

This FPGA routine is a modified version of a FPGA routine used previously on the final year project of D. Drennan. Written in VHDL, the modified routine is different in the following aspects:

- Error feedbacks' implemented.
- Fundamental frequency clock modified.
- Resetting of FPGA after error signal.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

ENTITY vector_gen is
    PORT (  address                 : IN std_logic_vector(3 downto 0);          -- address bus
            cs0                     : IN std_logic;
            -- chip select 0
            cs1                     : IN std_logic;
            -- chip select 1
            nrd                     : IN std_logic;
            -- not read
            nwe                     : IN std_logic;
            -- not write en
            clk                     : IN std_logic;
            -- clock
            data                    : IN std_logic_vector(9 downto 0);          -- data bus
            pwm_sync_in1            : IN std_logic;
    -- pwm sync in 1
            pwm_sync_in2            : IN std_logic;
    -- pwm sync in 1
            npwm_disable1           : IN std_logic;
    -- not pwm disable 1
            npwm_disable2           : IN std_logic;
    -- not pwm disable 2
            pwm_err1                : IN std_logic_vector(8 downto 0);  -- pwm error 1
            pwm_err2                : IN std_logic_vector(8 downto 0);  -- pwm error 2
            dis_protection          : IN std_logic;
    -- dip1
            err_polarity            : IN std_logic;
    -- dip2
            pwm_top1                : OUT std_logic_vector(3 downto 0);         -- top PWM 1
            pwm_bot1                : OUT std_logic_vector(3 downto 0); -- bottom PWM 1
            pwm_top2                : OUT std_logic_vector(3 downto 0);         -- top PWM 2
            pwm_bot2                : OUT std_logic_vector(3 downto 0); -- bottom PWM 2
            dcdump1                 : OUT std_logic;
            dcdump2                 : OUT std_logic;
            compare1                : OUT std_logic_vector(1 downto 0);
            compare2                : OUT std_logic_vector(1 downto 0);
            do                      : OUT std_logic_vector(8 downto 0);
            pwm_error1              : OUT std_logic;
            pwm_error2              : OUT std_logic;
            ramp_dir1               : OUT std_logic;                                --
```

```
ramp direction for
                        ramp_dir2           : OUT std_logic);                    -- end
of cycle poll
    end entity vector_gen;

    architecture ver1 of vector_gen is

    -- Phase signals
    type phase_arm                          is (zero,pos,neg,dead01,dead02,dead12);
    signal A                                    : phase_arm;
    signal B                                    : phase_arm;
    signal C                                    : phase_arm;
    signal A_con                            : std_logic_vector(1 downto 0);
    signal B_con                            : std_logic_vector(1 downto 0);
    signal C_con                            : std_logic_vector(1 downto 0);
    -- Timing signals
    signal slow_clk                         : std_logic;                         --
slower clock
    signal cnt                                  : integer range 0 to 2**10;          --
clock hard coded
    type timer                                  is (D1,D2,D3);
    signal time_state                   : timer;                             --
timer states
    signal D1_cnt                           : integer range 0 to 2**10;      -- end state 1
timer
    signal D2_cnt                           : integer range 0 to 2**10;      -- end state 2
timer
    -- State vector registers
    signal v1                                   : std_logic_vector(9 downto 0);  -- current vectors
    signal v2                                   : std_logic_vector(9 downto 0);  -- current vectors
    signal v3                                   : std_logic_vector(9 downto 0);  -- current vectors

    signal v1b,v2b,v3b                      : std_logic_vector(9 downto 0);  -- buffered vectors
    signal v1bb,v2bb,v3bb               : std_logic_vector(9 downto 0);  -- 2xbuffered vectors
    signal v1t,v2t                          : std_logic_vector(9 downto 0);  -- current times
    signal v1tb,v2tb                        : std_logic_vector(9 downto 0);  -- buffered times
    signal v1tbb,v2tbb                      : std_logic_vector(9 downto 0);  -- 2xbuffered times

    -- Tri state control
    signal tri_con                          : std_logic;

    -- AD
    signal pwm_error                    : std_logic;

    BEGIN
        pwm_error1 <= '0';
                -- not used
        pwm_error2 <= '0';
                -- not used
        compare1(1 downto 0) <= "00";                                            -- not
used
        compare2(1 downto 0) <= "00";                                            -- not
used
        dcdump1 <= '0';
                        -- not used
        dcdump2 <= '0';
                        -- not used
        tri_con <= '0';
```

```
do <= "111111111" when (tri_con = '1') else "ZZZZZZZZZ";                -- not used

pwm_top1(3) <= '0';
        -- turn off PWM 4
pwm_top2(3) <= '0';
pwm_bot1(3) <= '0';
pwm_bot2(3) <= '0';

-- Write data to buffers
process(clk)
begin
        if rising_edge(clk) then
                if (nwe = '0') then
                        if (cs0 = '1') then
                                case address is
                                        when "0000" =>
                                                v1bb <= data(9 downto 0);
                                        when "0001" =>
                                                v2bb <= data(9 downto 0);
                                        when "0010" =>
                                                v3bb <= data(9 downto 0);
                                        when others =>
                                end case;
                        elsif (cs1 = '1') then
                                case address is
                                        when "0000" =>
                                                v1tbb <= data(9 downto 0);
                                        when "0001" =>
                                                v2tbb <= data(9 downto 0);
                                        when others =>
                                end case;
                        end if;
                end if;
        end if;
end process;

-- Timing function
process(clk)
        variable slow_clk                       : integer range 0 to 2**3;
begin
        if rising_edge(clk) then
                slow_clk := slow_clk + 1;
                if (slow_clk = 4) then
                        cnt <= cnt + 1;
                        slow_clk := 0;
                end if;
                if (cnt = 417) then
                        ramp_dir1 <= '0';
        -- set ramp direction
                        ramp_dir2 <= '0';
                end if;
                if (cnt = 833) then
                        ramp_dir1 <= '1';
        -- to comply with DSP
                        ramp_dir2 <= '1';
                        time_state <= D1;
        -- after cycle -> D0
                        cnt <= 0;
```

```
                -- reset counter
                        v1  <= v1b;
                -- move buffered vectors
                        v1b  <= v1bb;
                        v2  <= v2b;
                        v2b  <= v2bb;
                        v3  <= v3b;
                        v3b  <= v3bb;
                        v1t  <= v1tb;
                -- move buffered times
                        v1tb <= v1tbb;
                        v2t  <= v2tb;
                        v2tb <= v2tbb;
                        D1_cnt <= conv_integer(unsigned(v1tb));
                        D2_cnt <= conv_integer(unsigned(v1tb)) + conv_integer(unsigned(v2tb));
                elsif (cnt = D1_cnt) then
                        time_state <= D2;
                elsif (cnt = D2_cnt) then
                        time_state <= D3;
                end if;
                case time_state is
                        when D1 =>
                                A_con <= v1(5 downto 4);                                -- vec-
tor -> phase
                                B_con <= v1(3 downto 2);
                                C_con <= v1(1 downto 0);
                        when D2 =>
                                A_con <= v2(5 downto 4);                                -- vec-
tor -> phase
                                B_con <= v2(3 downto 2);
                                C_con <= v2(1 downto 0);
                        when D3 =>
                                A_con <= v3(5 downto 4);                                -- vec-
tor -> phase
                                B_con <= v3(3 downto 2);
                                C_con <= v3(1 downto 0);
                end case;
        end if;
end process;

-- Gating Pulses for Phase A
process(clk)
        variable dcnt_A         : integer range 0 to 2**7;
begin
        if rising_edge(clk) then
                case A is
                        when zero =>
-- zero state
                                dcnt_A := 0;
-- begin dcnt at zero
                                pwm_top1(0) <= '1' or pwm_error;
                                pwm_top2(0) <= '0' or pwm_error;
                                pwm_bot1(0) <= '0' or pwm_error;

                                pwm_bot2(0) <= '1' or pwm_error;
                                if (A_con = "01") then
                                        A <= dead01;
                                elsif (A_con = "10") then
```

```
                                        A <= dead02;
                                end if;
                        when pos =>
                -- positive state
                                pwm_top1(0) <= '0' or pwm_error;
                                pwm_top2(0) <= '0' or pwm_error;
                                pwm_bot1(0) <= '1' or pwm_error;
                                pwm_bot2(0) <= '1' or pwm_error;
                                if (A_con = "00") then
                                        A <= dead01;
                                elsif (A_con = "10") then
                                        A <= dead12;
                                end if;
                        when neg =>
                -- negative state
                                pwm_top1(0) <= '1' or pwm_error;
                                pwm_top2(0) <= '1' or pwm_error;
                                pwm_bot1(0) <= '0' or pwm_error;
                                pwm_bot2(0) <= '0' or pwm_error;
                                if (A_con = "00") then
                                        A <= dead02;
                                elsif (A_con = "01") then
                                        A <= dead12;
                                end if;
                        when dead01 =>
        -- dead time zero to pos
                                pwm_top1(0) <= '1' or pwm_error;
                                pwm_top2(0) <= '0' or pwm_error;
                                pwm_bot1(0) <= '1' or pwm_error;
                                pwm_bot2(0) <= '1' or pwm_error;
                                if (dcnt_A > 124) then                          --
dead time = 5us
                                        dcnt_A := 0;
                                        if (A_con = "00") then
                                                A <= zero;
                                        elsif (A_con = "01") then
                                                A <= pos;
                                        else
                                                A <= dead12;
                                        end if;
                                end if;
                                dcnt_A := dcnt_A + 1;
                        when dead02 =>
        -- dead time zero to neg
                                pwm_top1(0) <= '1' or pwm_error;
                                pwm_top2(0) <= '1' or pwm_error;
                                pwm_bot1(0) <= '0' or pwm_error;
                                pwm_bot2(0) <= '1' or pwm_error;
                                if (dcnt_A > 124) then
                                        dcnt_A := 0;
                                        if (A_con = "00") then
                                                A <= zero;
                                        elsif (A_con = "10") then
                                                A <= neg;
                                        else
                                                A <= dead12;
                                        end if;
                                end if;
```

```
                                        dcnt_A := dcnt_A + 1;
                                when dead12 =>
-- dead time pos to neg
                                        pwm_top1(0) <= '1' or pwm_error;
                                        pwm_top2(0) <= '1' or pwm_error;
                                        pwm_bot1(0) <= '1' or pwm_error;
                                        pwm_bot2(0) <= '1' or pwm_error;
                                        if (dcnt_A > 124) then
                                                dcnt_A := 0;
                                                if (A_con = "00") then
                                                        A <= zero;
                                                elsif (A_con = "01") then
                                                        A <= pos;
                                                else
                                                        A <= neg;
                                                end if;
                                        end if;
                                        dcnt_A := dcnt_A + 1;
                        end case;
        end if;
end process;

-- Gating Pulses for Phase B
process(clk)
        variable dcnt_B         : integer range 0 to 2**7;
begin
        if rising_edge(clk) then
                        case B is
                                when zero =>
-- zero state
                                        dcnt_B := 0;
-- begin dcnt at zero (double check)
                                        pwm_top1(1) <= '1' or pwm_error;
                                        pwm_top2(1) <= '0' or pwm_error;
                                        pwm_bot1(1) <= '0' or pwm_error;
                                        pwm_bot2(1) <= '1' or pwm_error;
                                        if (B_con = "01") then
                                                B <= dead01;
                                        elsif (B_con = "10") then
                                                B <= dead02;
                                        end if;
                                when pos =>
        -- positive state
                                        pwm_top1(1) <= '0' or pwm_error;
                                        pwm_top2(1) <= '0' or pwm_error;
                                        pwm_bot1(1) <= '1' or pwm_error;
                                        pwm_bot2(1) <= '1' or pwm_error;
                                        if (B_con = "00") then
                                                B <= dead01;
                                        elsif (B_con = "10") then
                                                B <= dead12;
                                        end if;
                                when neg =>
        -- negative state
                                        pwm_top1(1) <= '1' or pwm_error;
                                        pwm_top2(1) <= '1' or pwm_error;
                                        pwm_bot1(1) <= '0' or pwm_error;
                                        pwm_bot2(1) <= '0' or pwm_error;
```

```
                                        if (B_con = "00") then
                                                B <= dead02;
                                        elsif (B_con = "01") then
                                                B <= dead12;
                                        end if;
                                when dead01 =>
-- dead time zero to pos
                                        pwm_top1(1) <= '1' or pwm_error;
                                        pwm_top2(1) <= '0' or pwm_error;
                                        pwm_bot1(1) <= '1' or pwm_error;
                                        pwm_bot2(1) <= '1' or pwm_error;
                                        if (dcnt_B > 124) then
                                                dcnt_B := 0;
                                                if (B_con = "00") then
                                                        B <= zero;
                                                elsif (B_con = "01") then
                                                        B <= pos;
                                                else
                                                        B <= dead12;
                                                end if;
                                        end if;
                                        dcnt_B := dcnt_B + 1;
                                when dead02 =>
-- dead time zero to neg
                                        pwm_top1(1) <= '1' or pwm_error;
                                        pwm_top2(1) <= '1' or pwm_error;
                                        pwm_bot1(1) <= '0' or pwm_error;
                                        pwm_bot2(1) <= '1' or pwm_error;
                                        if (dcnt_B > 124) then
                                                dcnt_B := 0;
                                                if (B_con = "00") then
                                                        B <= zero;
                                                elsif (B_con = "10") then
                                                        B <= neg;
                                                else
                                                        B <= dead12;
                                                end if;
                                        end if;
                                        dcnt_B := dcnt_B + 1;
                                when dead12 =>
-- dead time pos to neg
                                        pwm_top1(1) <= '1' or pwm_error;
                                        pwm_top2(1) <= '1' or pwm_error;
                                        pwm_bot1(1) <= '1' or pwm_error;
                                        pwm_bot2(1) <= '1' or pwm_error;
                                        if (dcnt_B > 124) then
                                                dcnt_B := 0;
                                                if (B_con = "00") then
                                                        B <= zero;
                                                elsif (B_con = "01") then
                                                        B <= pos;
                                                else
                                                        B <= neg;
                                                end if;
                                        end if;
                                        dcnt_B := dcnt_B + 1;
                        end case;
                end if;
```

```
end process;

-- Gating Pulses for Phase C
process(clk)
        variable dcnt_C                 : integer range 0 to 2**7;
begin
        if rising_edge(clk) then
                        case C is
                                when zero =>
-- zero state
                                        dcnt_C := 0;
-- begin dcnt at zero (double check)
                                        pwm_top1(2) <= '1' or pwm_error;
                                        pwm_top2(2) <= '0' or pwm_error;
                                        pwm_bot1(2) <= '0' or pwm_error;
                                        pwm_bot2(2) <= '1' or pwm_error;
                                        if (C_con = "01") then
                                                C <= dead01;
                                        elsif (C_con = "10") then
                                                C <= dead02;
                                        end if;
                                when pos =>
        -- positive state
                                        pwm_top1(2) <= '0' or pwm_error;
                                        pwm_top2(2) <= '0' or pwm_error;
                                        pwm_bot1(2) <= '1' or pwm_error;
                                        pwm_bot2(2) <= '1' or pwm_error;
                                        if (C_con = "00") then
                                                C <= dead01;
                                        elsif (C_con = "10") then
                                                C <= dead12;
                                        end if;
                                when neg =>
        -- negative state
                                        pwm_top1(2) <= '1' or pwm_error;
                                        pwm_top2(2) <= '1' or pwm_error;
                                        pwm_bot1(2) <= '0' or pwm_error;
                                        pwm_bot2(2) <= '0' or pwm_error;
                                        if (C_con = "00") then
                                                C <= dead02;
                                        elsif (C_con = "01") then
                                                C <= dead12;
                                        end if;
                                when dead01 =>
-- dead time zero to pos
                                        pwm_top1(2) <= '1' or pwm_error;
                                        pwm_top2(2) <= '0' or pwm_error;
                                        pwm_bot1(2) <= '1' or pwm_error;
                                        pwm_bot2(2) <= '1' or pwm_error;
                                        if (dcnt_C > 124) then
                                                dcnt_C := 0;
                                                if (C_con = "00") then
                                                        C <= zero;
                                                elsif (C_con = "01") then
                                                        C <= pos;
                                                else
                                                        C <= dead12;
                                                end if;
```

```
                                        end if;
                                        dcnt_C := dcnt_C + 1;
                                when dead02 =>
        -- dead time zero to neg
                                        pwm_top1(2) <= '1' or pwm_error;
                                        pwm_top2(2) <= '1' or pwm_error;
                                        pwm_bot1(2) <= '0' or pwm_error;
                                        pwm_bot2(2) <= '1' or pwm_error;
                                        if (dcnt_C > 124) then
                                                dcnt_C := 0;
                                                if (C_con = "00") then
                                                        C <= zero;
                                                elsif (C_con = "10") then
                                                        C <= neg;
                                                else
                                                        C <= dead12;
                                                end if;
                                        end if;
                                        dcnt_C := dcnt_C + 1;
                                when dead12 =>
        -- dead time pos to neg
                                        pwm_top1(2) <= '1' or pwm_error;
                                        pwm_top2(2) <= '1' or pwm_error;
                                        pwm_bot1(2) <= '1' or pwm_error;
                                        pwm_bot2(2) <= '1' or pwm_error;
                                        if (dcnt_C > 124) then
                                                dcnt_C := 0;
                                                if (C_con = "00") then
                                                        C <= zero;
                                                elsif (C_con = "01") then
                                                        C <= pos;
                                                else
                                                        C <= neg;
                                                end if;
                                        end if;
                                        dcnt_C := dcnt_C + 1;
                                end case;
                        end if;
        end process;

    -- AD
        process(clk,pwm_err1,pwm_err2)
        begin
                if clk'event and clk='1' then
                        if (pwm_err1(7 downto 2) /= "111111") or (pwm_err2(7 downto 2) /= "111111") then
                                pwm_error <= '1';
                        end if;
                end if;
        end process;

end architecture ver1;
```

Appendix E MATLAB® Files

E.1 Current and Voltage %THD Calculations

```
close all;
clear;

ac        =   loadcsv('tek00007.csv');   % loading relevant tek.csv file
(40ms long)
ac(:,2)   =   1*ac(:,2);         % Scaling the magnitudes (*x)

f         =   [0:length(ac)-1]/length(ac)/(ac(2,1)-ac(1,1));

% creating a 1*10000 matrix to zero 50Hz & DC fft components
n         =   [ 0*ones(1,1); 1*ones(1,1); 0*ones(1,1); 1*ones(1,1);
                1.0*ones(10000-4,1); ];

% creating a 1*10000 matrix to zero 50Hz & DC fft components
d         =   [ 0*ones(1,1); 1*ones(1,1); 1*ones(1,1); 1*ones(1,1);
                1.0*ones(10000-4,1); ];


f_ac            =   abs(fft(ac(:,2)))/10000;      %fft of current values in
idc (column 2)
f_ac_n          =   n.*f_ac;                      %Removing 50Hz & DC compo-
nent from numerator
f_ac_d          =   d.*f_ac;                      %Removing DC component from
denominator


figure(1);
plot(ac(:,1),ac(:,2));
%bar(f,f_npcc);
%figure(2);
%bar(f,d,'r');
%figure(3);
%bar(f,n,'r');
figure(4);
bar(f,f_ac_n);
figure(5);
bar(f,f_ac_d);


THD    =    sqrt( ((sum(f_ac_n(1:length(f_ac_n)/2).^2))*sqrt(2)) /
((sum(f_ac_d(1:length(f_ac_d)/2).^2))*sqrt(2)) )*100
```

E.2 Efficiency Calculations

E.2.1 AC Power Calculations

```
close all;
clear;

ia  =   loadcsv('tek00001.csv');    %Loading 20ms A-Phase Current waveform
figure(1);
```

```
plot(ia(:,1),ia(:,2));                  %plotting waveform

va    =    loadcsv('tek00004.csv');     %Loading  20ms A-Phase Voltage waveform
figure(2);
plot(va(:,1),va(:,2));                  %plotting waveform

ib    =    loadcsv('tek00002.csv');     %Loading  20ms B-Phase Current waveform
figure(3);
plot(ib(:,1),ib(:,2));                  %plotting waveform

vb    =    loadcsv('tek00005.csv');     %Loading  20ms B-Phase Voltage waveform
figure(4);
plot(vb(:,1),vb(:,2));                  %plotting waveform

ic    =    loadcsv('tek00003.csv');     %Loading  20ms C-Phase Current waveform
figure(5);
plot(ic(:,1),ic(:,2));                  %plotting waveform

vc    =    loadcsv('tek00006.csv');     %Loading  20ms C-Phase Voltage waveform
figure(6);
plot(vc(:,1),vc(:,2));                  %plotting waveform

% calculating AC power, multiplying each point within voltage array by its
% corresponding value in current array
p    =    va .* ia + vb .* ib + vc .* ic;
figure(7);
plot(p);

P    =    mean(p);
sprintf( 'Pac = %12.3f kW\n', mean(p)/1000 )
```

E.2.2 DC Power Calculations

```
close all;
clear;

i    =    loadcsv('tek00000.csv');     %Loading 20ms DC Current Measurement
i    =    20/10e-3*i;
figure(1);
plot(i(:,1),i(:,2));                    %plotting I waveform

figure(2);
p    =    800.*i(:,2);                 %Multiplying DC voltage with Measured
DC Current
plot(p);

sprintf( 'Pdc = %12.3f kW', mean(p)/1000 ) %obtaining mean DC power
```

E.3 DC Capacitor Power Loss Calculations

```
close all;
clear;

idc   =    loadcsv('tek00000.csv');     % loading relevant tek.csv file
idc(:,2)    =    100*idc(:,2);          % Scaling the current magnitudes (*100)

f          =    [0:length(idc)-1]/length(idc)/(idc(2,1)-idc(1,1));
```

```
            % creating a 1*10000 scaling Array for the ESR derating as the
frequency increases
c       =   [ 0*ones(2,1); 1*ones(1,1); 0.851*ones(1,1); 0.69*ones(1,1);
            0.648*ones(1,1); 0.606*ones(1,1); 0.564*ones(1,1);
0.523*ones(1,1);
            0.510*ones(1,1); 0.497*ones(1,1); 0.484*ones(1,1);
0.471*ones(1,1);
            0.463*ones(1,1); 0.454*ones(1,1); 0.446*ones(1,1);
0.438*ones(1,1);
            0.435*ones(2,1); 0.432*ones(4,1); 0.419*ones(4,1);
0.413*ones(4,1);
            0.406*ones(4,1); 0.400*ones(4,1); 0.395*ones(22,1);
0.380*ones(22,1);
            0.374*ones(22,1); 0.367*ones(4895,1);   % for rest of half of
the fft distribution ((10000points)/2 -105)
            0.0*ones(10000-5000,1); ];              % zero last half of ma-
trix (10000points)/2

h       =   [1*ones(5000,1); 0.0*ones(10000-5000,1);];

f_idc           =   abs(fft(idc(:,2)))/10000;   %fft of current values in
idc (column 2)
f_idc_rms       =   f_idc/sqrt(2);              %RMS value of current in
fft
f_idc_rms_h     =   h.*f_idc/sqrt(2);           %displays half of RMS fft

r       =   0.015;                      %ESR @ 50Hz (from datasheets)
w_r     =   c.*r;                       %ESR weighted with frequency (from
datasheets)

figure(1);
plot(idc(:,1),idc(:,2));
%bar(f,f_npcc);
figure(2);
bar(f,c,'r');
figure(3);
bar(f,w_r,'r');
figure(10);
bar(f,f_idc_rms_h);

P_L_idc  = sum(w_r.*((f_idc_rms_h).^2))  %sum of I^2*R values
```

E.4 Inductor Ripple THD calculations

```
close all;
clear;

ac      =   loadcsv('tek00002.csv');    % loading relevant tek.csv file
ac(:,2) =   1*ac(:,2);          % Scaling the magnitudes (*x)

f       =   [0:length(ac)-1]/length(ac)/(ac(2,1)-ac(1,1));

    % creating a 1*10000 scaling matrix for the ESR derating as the fre-
    quency increases

n       =   [ 0*ones(1,1); 1*ones(1,1); 0*ones(1,1); 1*ones(1,1);
              1.0*ones(10000-4,1); ];
                        % zero last half of matrix (10000points)/2

d       =   [ 0*ones(1,1); 1*ones(1,1); 1*ones(1,1); 1*ones(1,1);
```

```
                1.0*ones(10000-4,1); ];
                        % zero last half of matrix (10000points)/2

%h        =    [1*ones(5000,1); 0.0*ones(10000-5000,1);];


f_ac             =    abs(fft(ac(:,2)))/10000;
                  %fft of current values in idc (column 2)

f_ac_n           =    n.*f_ac;
f_ac_d           =    d.*f_ac;

%f_idc_rms        =    f_idc/sqrt(2);       %RMS value of current in fft
%f_idc_rms_h      =    h.*f_idc/sqrt(2);    %displays half of RMS fft

%r        =    0.015;          %ESR @ 50Hz (from datasheets)
%w_r      =    c.*r;           %ESR weighted with frequency (from datasheets)


figure(1);
plot(ac(:,1),ac(:,2));
%bar(f,f_npcc);
%figure(2);
%bar(f,d,'r');
%figure(3);
%bar(f,n,'r');
figure(4);
bar(f,f_ac_n);
figure(5);
bar(f,f_ac_d);

THD    =    sqrt( ((sum(f_ac_n(1:length(f_ac_n)/2).^2))*sqrt(2)) /
((sum(f_ac_d(1:length(f_ac_d)/2).^2))*sqrt(2)) )*100
```